



LITELINK™ - CPC5604

Optical Data Access Arrangement Circuit

Application Note

January, 2000

Contents

1.0	Introduction	1
2.0	Architecture	2
2.1	Package Drawing	2
2.2	Pin Definitions and Functions	2
2.3	Block Diagram	3
2.4	Receive Signal Path	4
2.5	Transmit Signal Path	5
2.6	Ring Signal Detection	5
2.7	Caller ID Protection	6
3.0	DC Characteristics	7
3.1	On-Hook Resistance	7
3.2	Current Limiting	7
3.3	CTR-21	8
4.0	AC Characteristics	8
4.1	Differential and Single Ended Mode	8
4.2	Receive and Transmit Frequency Response	8
4.3	Distortion	11
4.4	Trans-Hybrid loss	13
4.5	Return Loss	14
4.6	Snoop Mode Frequency Response	15
4.7	Snoop Mode Distortion	16
4.8	Snoop Mode Common Mode Rejection Ratio (CMRR)	17
5.0	Applications	18
5.1	North American Reference Design Schematic	18
5.2	North American Reference Design Bill of Materials	19
5.3	International Reference Design Schematic	20
5.4	International Reference Design Bill of Materials	21
5.5	CTR-21 Reference Design Schematic	22
5.6	CTR-21 Reference Design Bill of Materials	23
5.7	CTR-21 with Exceptions Reference Design Schematic	24
5.8	CTR-21 with Exceptions Reference Design Bill of Materials	25
5.9	Country Specific Component Values	26
5.10	Interconnection to Rockwell 56K Chipset	27
5.11	Interconnection to Lucent 56K Chipset	28

LITELINK™ (CPC5604)

Optical Data Access Arrangement Circuit

1.0 INTRODUCTION

CP Clare's LITELINK™ (CPC5604) is a single package DAA solution that can be used for a variety of telephone line interface applications including high performance 56kbps modems. The LITELINK™ is an advanced integrated circuit that uses optical signal coupling techniques to provide the required electrical isolation between telephone line and the user's host circuitry. The LITELINK™ differs from other DAA solutions using either optical or capacitive isolation techniques by including the barrier inside the IC package which eliminates the need for external high voltage capacitors or optocouplers in the data path, thus saving board space and eliminating cost. The LITELINK™ has been designed to meet or exceed the requirements of international regulatory agencies.

The key features of the LITELINK™ DAA are as follows:

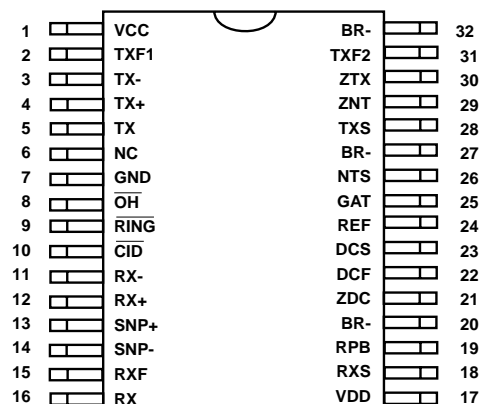
- Full differential or single ended transmit and receive signal coupling from the telephone line to the host system
- High voltage (1500 V_{RMS}) isolation between telephone line and host
- Ring signal detection
- Caller ID signal detection
- Hookswitch function
- Internal 2-4 wire converter
- Low power consumption
- Flat frequency response 30-4000Hz
- Low THD -80dB
- Minimum number of external components required
- Programmable International solution with CPC5601B chip
- PC Card compatible
- Current Limiting

For international PTT compliance, external passive components can be changed to meet different country requirements. Using the LITELINK™ in conjunction with the CPC5601 driver, will offer a software programmable solution using a digital serial interface to the host's microcontroller.

See CPC5601 Data Sheet for details on software programmable solutions.

2.0 ARCHITECTURE

2.1 Package Drawing



2.2 Pin Definitions and Functions

Pin #	Name	Function
1	V _{CC}	Host power supply, +5 Volts +/-5%.
2	TXF1	TX isolation amplifier output.
3	TX -	NEG differential transmit signal into DAA.
4	TX+	POS differential transmit signal into DAA.
5	TX	TX differential amplifier input.
6	NC	Not connected.
7	GND	Connect to host analog ground.
8	OH	Driving this signal low asserts the off-hook condition
9	RING	Active low indicates an incoming half waved ring signal ulsed High to Low at the ring frequency-typically 20Hz.
10	CID	Driving this signal low places the Caller ID information on the RX pins when the DAA is on hook (OH is de-asserted).
11	RX-	NEG differential analog receive signal from the telephone line and must be AC coupled with a 0.1uF capacitor.
12	RX+	POS differential analog receive signal from the telephone line and must be AC coupled with a 0.1uF capacitor.
13	SNP+	One of two differential snoop inputs.
14	SNP-	One of two differential snoop inputs.
15	RXF	Receive photodiode amplifier output.
16	RX	Receive photoamplifier summing junction.
17	V _{DD}	Power supply for line side portion of CPC5604.
18	RXS	Receive photodiode servo input.
19	RPB	Sets receive LED prebias current.
20	BR-	Return to bridge rectifier negative output.
21	ZDC	Sets electronic inductor DCR/Current Limit.
22	DCF	DC Filter point.
23	DCS	VI slope control via external resistor.
24	REF	1.25V internal voltage reference.
25	GAT	Depletion MOSFET gate control.
26	NTS	Receive signal input path via Tip and Ring.
27	BR-	Return to bridge rectifier negative output.
28	TXS	Receive photodiode amplifier input.
29	ZNT	Sets DAA impedance via external passive network.
30	ZTX	Transmit Transconductance gain setting pin.
31	TXF2	Receive photodiode amplifier output.
32	BR-	Return to bridge rectifier negative output.

North America

Tel: 800-CPCLARE
Fax: 978-524-4900

Europe

Tel: +32-11-300-868
Fax: +32-11-300-890

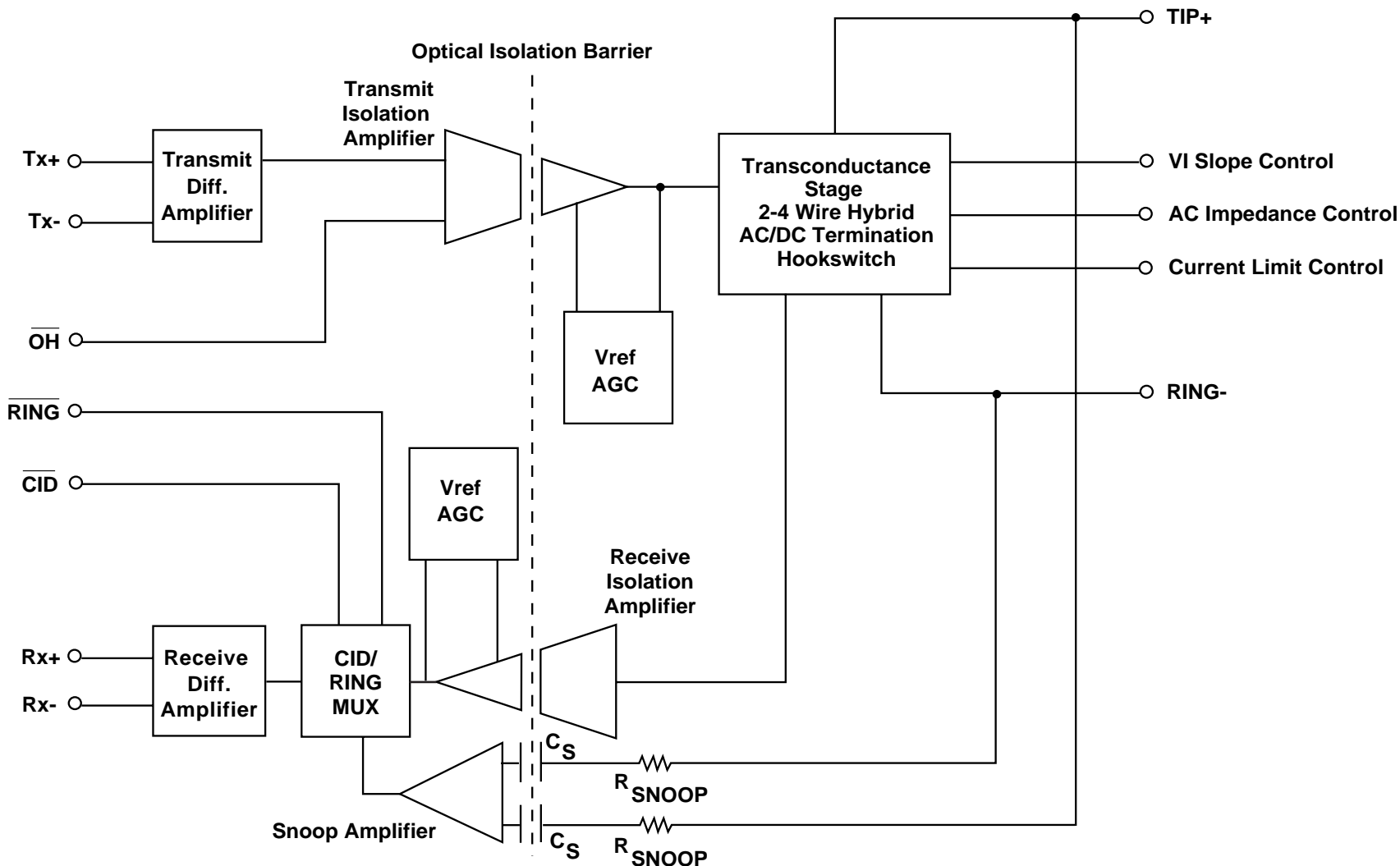
Asia

Tel: 886-2-2523-6368
Fax: 886-2-2523-6369

Japan

Tel: 03-3980-2212
Fax: 03-3980-2213

2.3 Block Diagram LITELINK™



2.4 Receive Signal Path (Refer to Block Diagram 2.3)

Signals to and from the telephone line to the LITELINK™ appear on Tip and Ring connections. The receive signal is extracted from the transmit signal via the 2-4 wire hybrid block. The receive signal is then converted to infrared light by the receive photodiode amplifier and LED front end. The intensity of the infrared light is modulated by the receive signal and this light is transferred across the electrical isolation barrier via reflective dome to a photodiode where the light is converted to a photocurrent. This photocurrent is a highly linear representation of the receive signal and is amplified and converted to a voltage. This single ended voltage is converted to a differential voltage signal where it is presented as RX+ and RX- and connects to the receive inputs of the host data pump.

Variations in gain due to quantum efficiency of the optics are virtually eliminated by an on chip AGC circuit which automatically sets the input to output gain of the photoamplifier to unity. This means that the receive signal on the telephone line is faithfully reproduced at the RX outputs in terms of amplitude to within 2dB of the received signal. Distortion at the RX outputs is -80dB maximum at a receive level of -3dB over the band of 30Hz-4kHz.

Single supply operation requires that the RX outputs be biased at 2.5V DC, therefore, it is necessary to use 0.1uF blocking capacitors for coupling the receive signal to the host. Figures 2.4.A and 2.4.B. illustrate connection to the host differentially and single ended respectively.

Figure 2.4.A Connection To Host Differential (Receive)

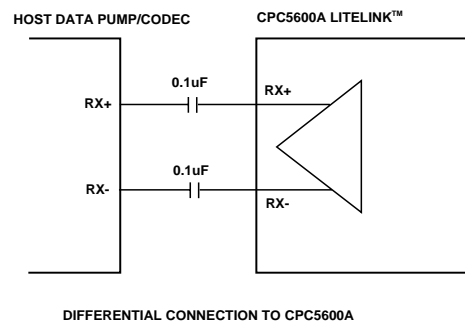
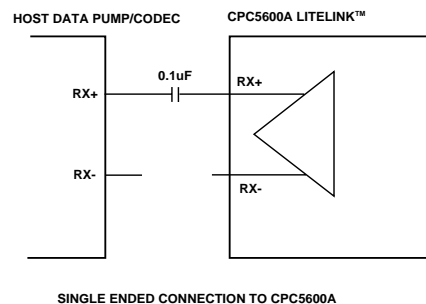


Figure 2.4.B Connection To Host Single Ended (Receive)



2.5 Transmit Signal Path
(Refer to Block Diagram 2.3)

Signals that are to be sent from the host to the telephone line are placed differentially on TX+ and TX-. The maximum value of the transmit signal should not exceed 0dBm or 2.18Vpp. The differential transmit signal is converted to a single ended signal by the LITELINK™. This signal is coupled to the transmit photodiode amplifier in a similar manner to the receive path.

At the output of this amplifier the voltage signal is coupled to a voltage to current converter via a transconductance stage where the transmit signal modulates the telephone line loop current. As in the receive stage, the gain of the transmit photodiode amplifier is set to unity automatically thereby limiting insertion loss to 0±1dB. Figure 2.5.A and 2.5.B illustrate connection to the host differentially and single ended respectively.

Figure 2.5.A Connection To Host Differential (Transmit)

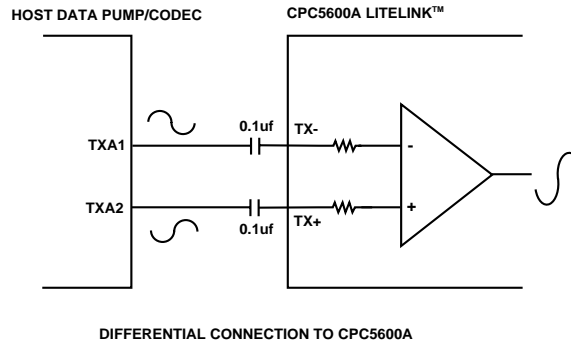
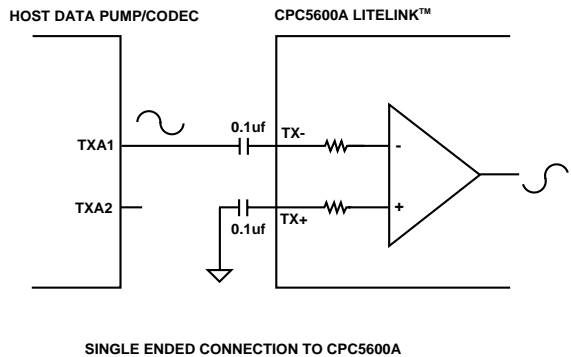


Figure 2.5.B Connection To Host Single Ended (Transmit)



2.6 Ring Signal Detection

The snoop circuit actively monitors the telephone line for 2 conditions:

1. Incoming ring signal
2. Caller ID information

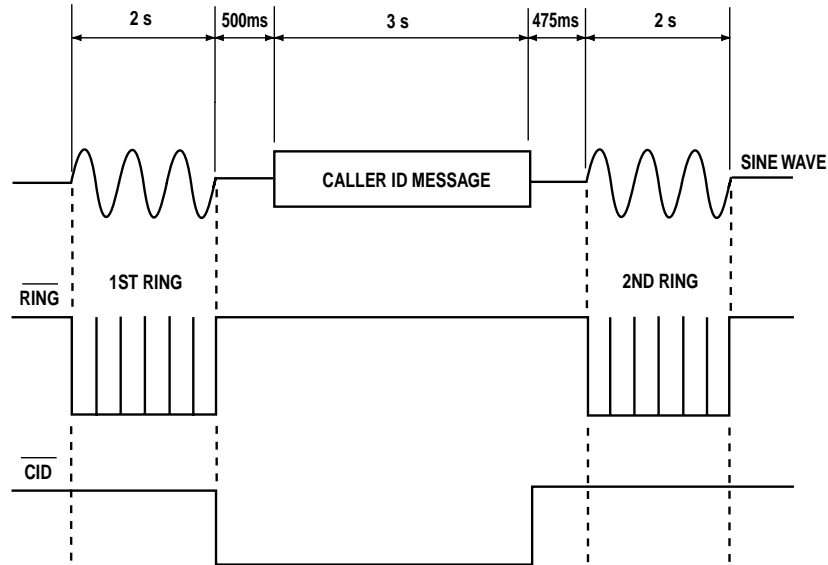
The Snoop circuit “snoops” the line continuously while the LITELINK™ is in the on-hook mode. Current taken from the telephone line in the on-hook condition by the LITELINK™ is maintained at a low 2uA maximum thus meeting regulatory requirements for minimum on-hook impedance limitation. When the central office places the ring signal on the telephone line, that signal is coupled through a pair of RC circuits to a differential amplifier in the LITELINK™.

Referring to Block Diagram 2.3, snoop capacitors connected to the SNP1/SNP2 pins provide a high voltage isolation barrier between the host and the telephone line while coupling the AC signals to the snoop amplifier. The ring signal is digitized and brought out to the RING pin where the host can qualify it as a valid ring signal.

The ring detection threshold is dependent on the values of 3 external components: R_{RXF} (R3), R_{SNOOP} (R5 or R6), and C_S (C6 or C7). The default values in the typical bill of materials reflects the parameters in the data sheet for typical operation. If it is desired to change the threshold, the values can be selected by using the equation: $V_{RING(PEAK)} = \left[\frac{330E-3}{5R_{RXF}} \right] \sqrt{\left(R_{SNOOP} \right)^2 + \frac{1}{(2\pi f C_S)^2}}$

Where f = ring frequency typically 20Hz.

Figure 2.7.A Caller ID Protocol



Care should be taken when using this equation since R_{RXF} (R3), C_S (C6 or C7), and R_{SNOOP} (R5 or R6) affect receive gain and Caller ID gain. It is recommended that R_{RXF} (R3) be set to the typical value and then after adjusting the ring detect threshold, check that CID gain is acceptable.

2.7 Caller ID Detection

Caller ID (CID) is a service offered by the telephone company to provide caller information (i.e. caller’s telephone number) to the called party. CID service is optional and signals only appear on the telephone lines of subscribers that pay for this feature. The CID information appears on the telephone line after the first ring burst is sent from the central office (CO).

Some of the characteristics of the CID signal are summarized below:

Parameter	Value
Signal Level	-13dBm
Link Type	Simplex, 2W
Transmission Scheme	Phase-coherent, FSK
Logical 1 (mark)	1200±12Hz
Logical 0 (Space)	2200± 22Hz
Transmission Rate	1200bps
Data	serial binary async
BER	< 10E -5
Bit Duration	833±50µS (same for start/stop as well)

Full details about the CID signal can be found in Bellcore document TR-TSY-000030, issue 1/1988.

Figure 2.7.A shows the CID timing diagram. Waveform #1 represents the Analog signals on the telephone line (amplitude not drawn to scale), waveform #2 is the digital RING detect output from the LITELINK™, waveform #3 is the CID input to the LITELINK™ from the Host. After the first ring burst is detected by the host, the host enables the CID line which automatically couples the snoop circuit to the RX outputs on the LITELINK™. This CID signal is then processed by the host and, after processing, the host will deactivate the CID signal. At this point the host can answer the call if desired by asserting the OH pin on the LITELINK™. It’s important to note that when the LITELINK™ goes off-hook, it automatically disconnects the snoop path from both the RX and RING outputs. Signals appearing on the telephone line are now coupled through the optical isolation barrier in the LITELINK™ and not via the capacitors in the snoop path.

CID gain from Tip and Ring to Rx+ and Rx- is determined by:

$$GAIN = \frac{10 R_{RXF}}{\sqrt{(R_{SNOOP})^2 + \frac{1}{(2\pi f C_S)^2}}}$$

Where f = CID signal frequency

For example, with $R_{RXF} = 75K\Omega$, $R_{SNOOP} = 1.4M\Omega$, $C_S = 220pF$, and $f = 600Hz$ calculated GAIN = 0.707 or a loss of -3dB at Rx+ and Rx-. This implies that the snoop frequency response is 600Hz. Gain is expressed in decibels by:

$$GAIN(db) = 20 \log \left[\frac{10 R_{RXF}}{\sqrt{(R_{SNOOP})^2 + \frac{1}{(2\pi f C_S)^2}}} \right]$$

3.0 DC CHARACTERISTICS

The LITELINK™ is designed to meet various country DC characteristics including the CTR-21 standard. The pins that control the VI characteristics and current limiting are designated ZDC and DCS. Meeting DC requirements are achieved by selecting the appropriate resistors R_{ZDC} (R16) and R_{DCS} (R20) respectively. Resistor values can also be switched in and out with the CPC5601 device or optocouplers which enables international compliance under software control. Suggested resistor values for various countries are listed in table 1. The VI profile on Tip and Ring is described by the following equation:

$$V_{LINE} = V_{BRIDGE} + \left[\frac{R_{DCS} + 12M\Omega}{R_{DCS}} \right] \left[0.5V + (I_{LINE} - 8mA)R_{ZDC} \right]$$

Example: I_{LINE} = 20mA, V_{BRIDGE} = 1.2V, R_{DCS} = 1.69MΩ, R_{ZDC} = 8Ω, V_{LINE} = 6.0V.

3.1 On-Hook Resistance

Figure 3.1.A shows the test setup for on-hook DC resistance. The battery is set to 100VDC and an ammeter is placed in series with the battery connection. When the DAA is in the on-hook state, the leakage current is obtained and then the battery voltage is divided by this current yielding the on-hook resistance. The LITELINK™ is guaranteed to have a leakage current < 10uA at 100V which is equivalent to an on-hook resistance > 10MΩ thus meeting regulatory approvals.

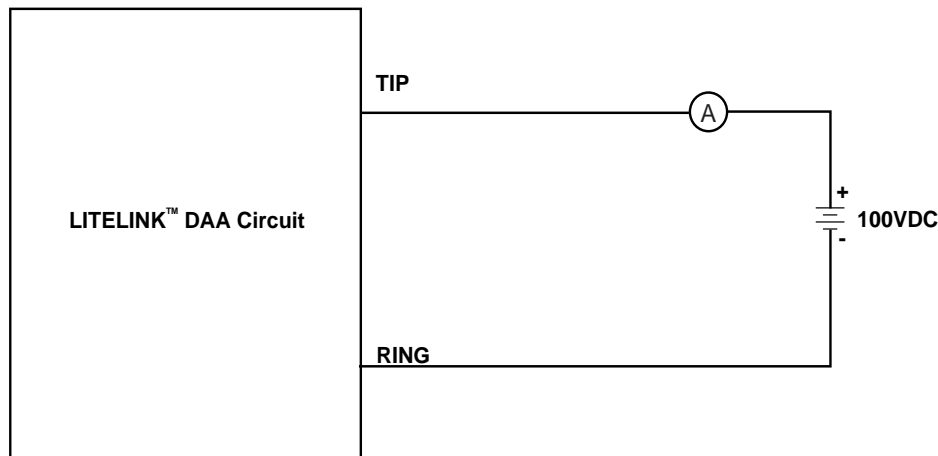
3.2 Current Limiting

The LITELINK™ includes a current limiting feature that is selectable via resistor R_{ZDC} (R16). The current limit value is set by the equation:

$$I_{LM} = \left[\frac{1V}{R_{ZDC}} \right] + 8mA$$

For US/Canada/Japan the recommended value for R_{ZDC} (R16) is 8Ω which yields a current limit value of 133mA. The current limiting feature is especially useful in the case where the host system is inadvertently connected to a digital PBX telephone port which usually has a very high current limit value. The current limiting capability will prevent damage to the LITELINK™ in this scenario.

Figure 3.1.A On-Hook DC Resistance Tip/Ring Setup



3.3 CTR-21 Compliance

CTR-21 is the standard for connection of data communications equipment to the European telephone network. The maximum current limit requirement in CTR-21 (Section 4.7.1) is 60mA and can be selected by the following equation:

$$I_{LM} = \left[\frac{1V}{R_{ZDC}} \right] + 8mA$$

CP Clare recommends current limit be set to 53mA using an R_{ZDC} value of 22Ω. Since VDD is regulated to +3.5V, excess power is dissipated in the external MOSFET package. Since the maximum off-hook line voltage and current in CTR-21 is 40V and 53mA respectively, the maximum power dissipated by the MOSFET is approximately 2.1W.

4.0 AC CHARACTERISTICS

In a similar manner to the DC characteristics, AC termination impedance is set via R_{ZNT} (R18). For North American applications and Japanese applications, a 604Ω resistor for R_{ZNT} (R18) is required to reflect 600Ω to the CO. For some other countries, complex termination is required in place of resistor R_{ZNT} (R18). Complex termination networks can be selected as a PCB stuffing option, jumpers, or all networks can be stuffed and selected via software by the CPC5601 programmable driver. Recommended values of R and C for each country are listed in Section 5.3.

4.1 Differential and Single Ended Mode

The LITELINK™ is designed to support either differential or single ended signals on Tx and/or Rx pins. The decision of which topology to use is based on the particular chipset being used to drive the LITELINK™. For example, most Lucent modem chips require both differential receive and transmit ability, while most Rockwell devices require differential transmit and single ended receive. The LITELINK™ supports a full 0dBm differential signal on its Tx inputs.

4.2 Receive and Transmit Frequency Response

Figures 4.2.A and 4.2.C show the test circuits for receive and transmit frequency response respectively. Figures 4.2.B and 4.2.D show the graphs for receive and transmit frequency response respectively.

Figure 4.2.A Receive Frequency Response Setup

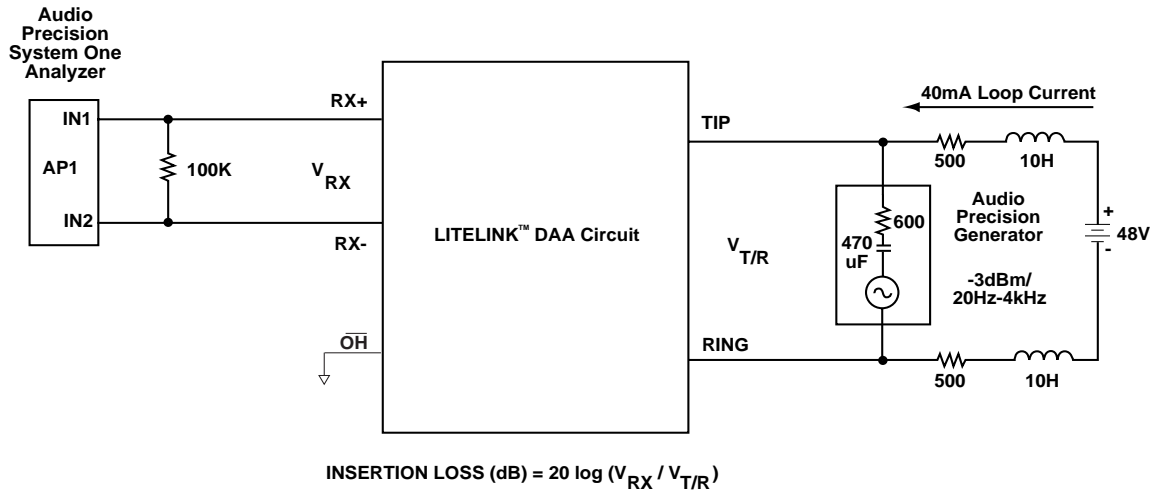


Figure 4.2.B Receive Frequency Response at Rx+

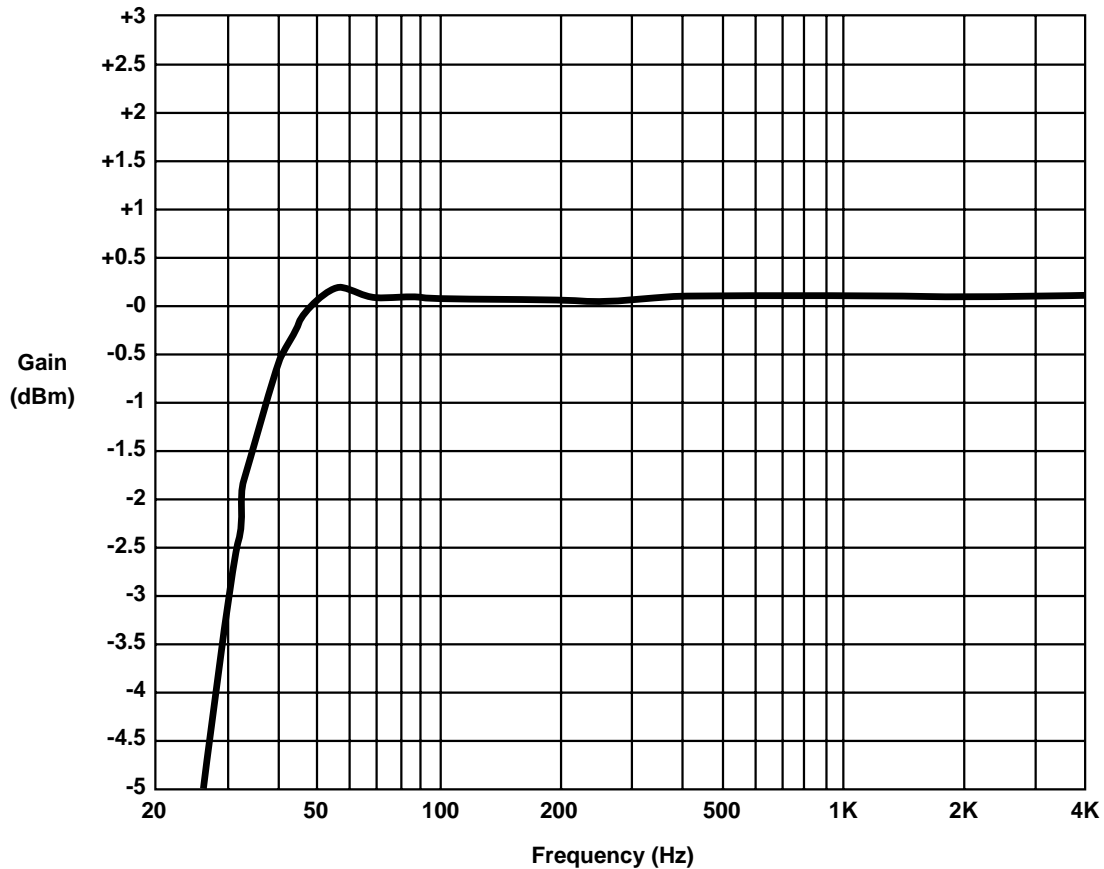


Figure 4.2.C Transmit Frequency Response Setup

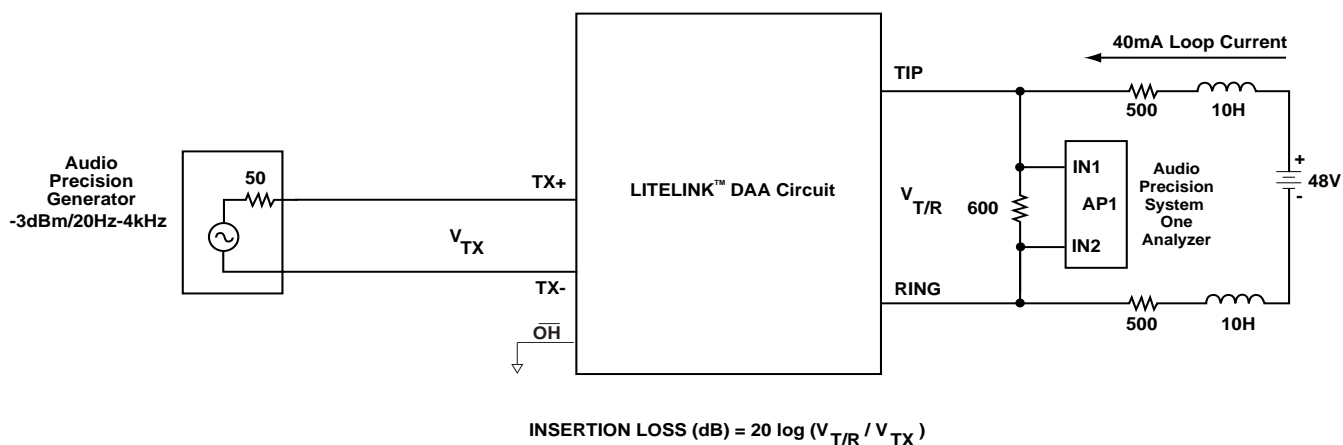
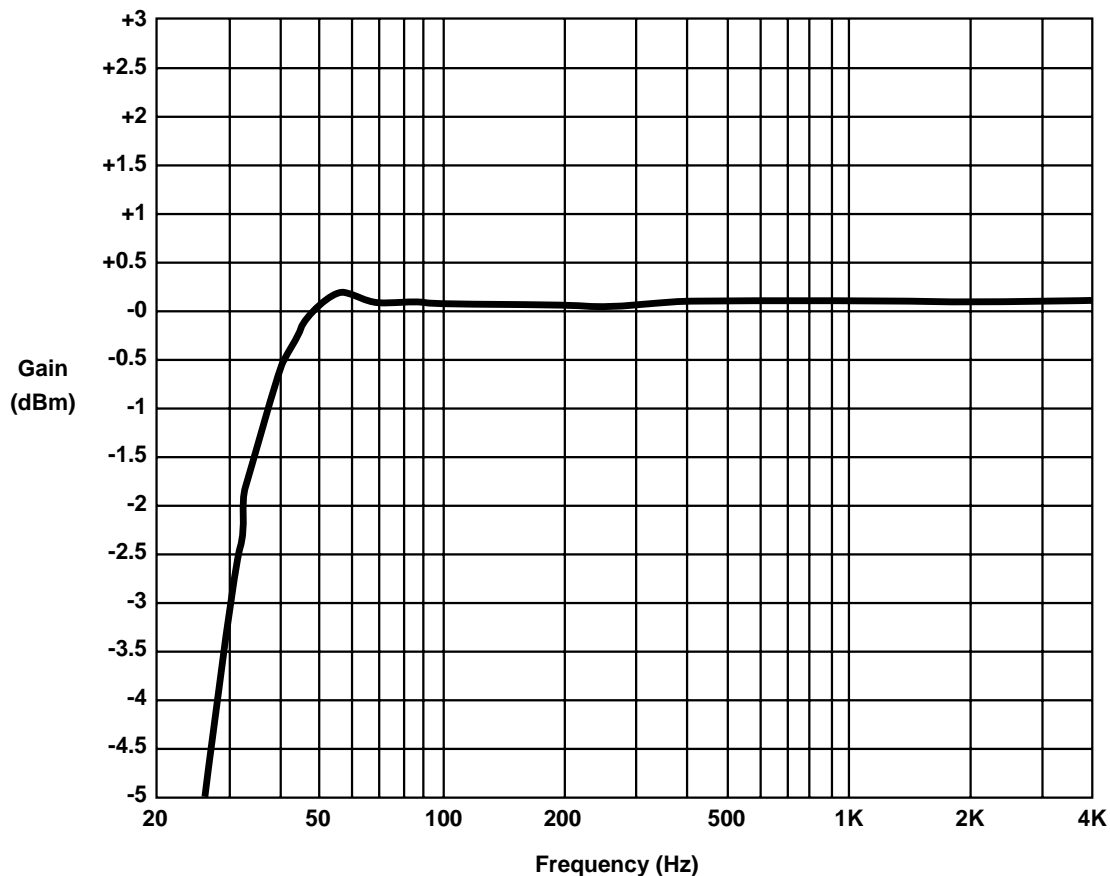


Figure 4.2.D Transmit Frequency Response Tx±



4.3 Distortion

Figures 4.3.A and 4.3.C show the test setup for receive and transmit distortion. Figures 4.3.B and 4.3.D show the THD at 600Hz graphs for receive and transmit respectively. Transmit signal for this test is set to -9dBm.

Figure 4.3.A Receive Distortion Test Tip/Ring to Rx± Setup

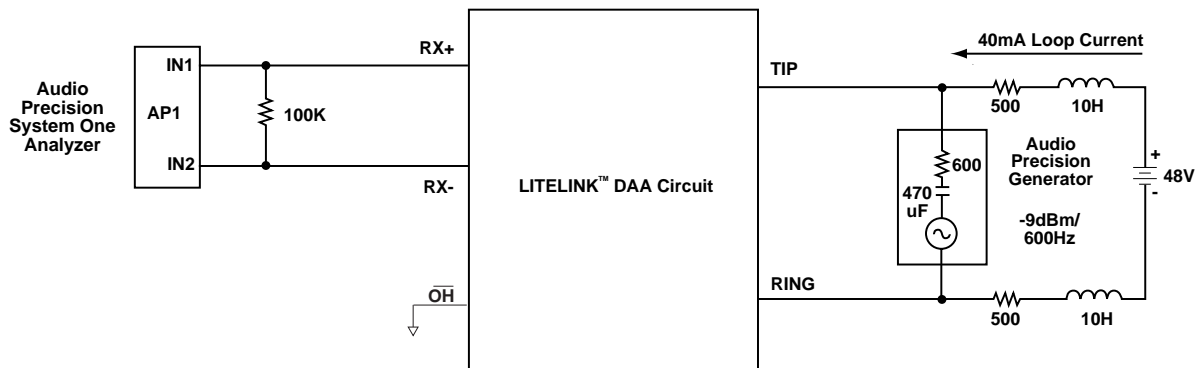


Figure 4.3.B Receive Distortion on Rx±

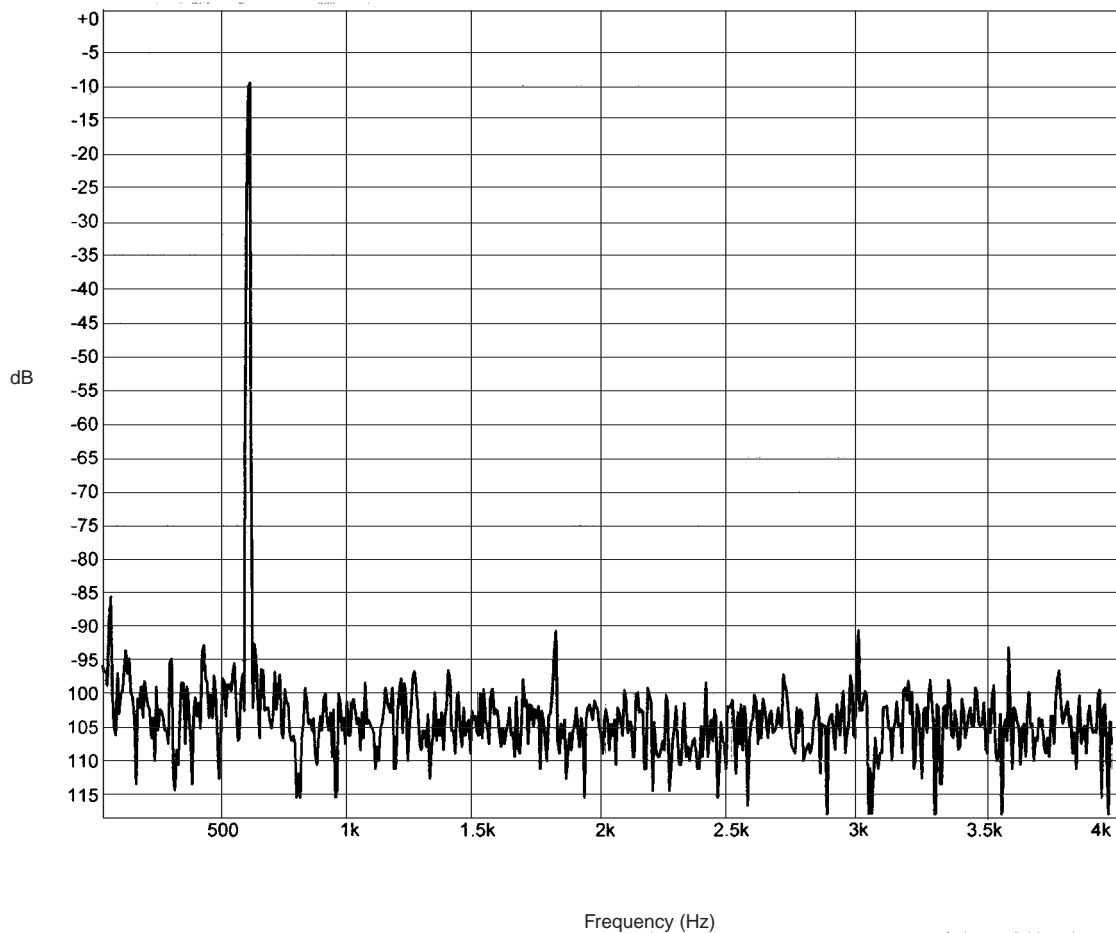


Figure 4.3.C Transmit Distortion Test Tx± to Tip/Ring Setup

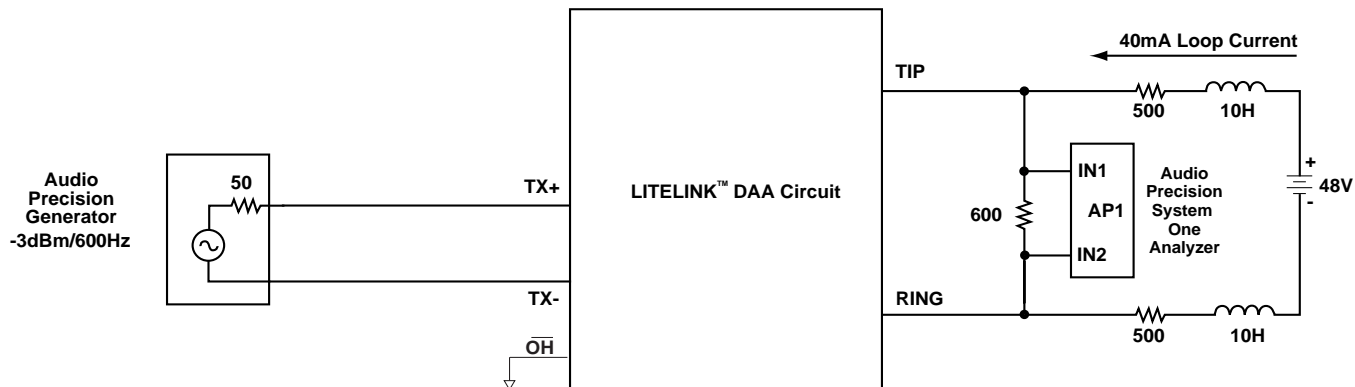
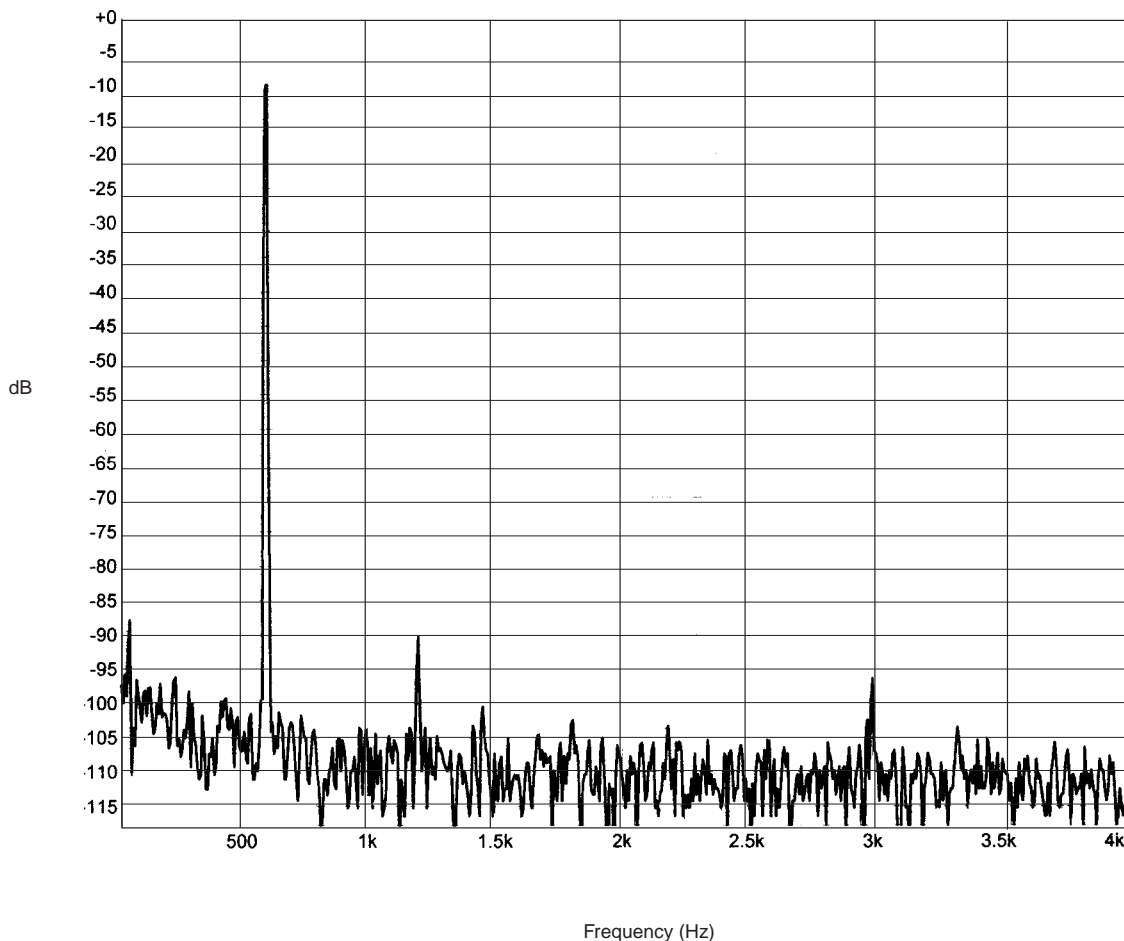


Figure 4.3.D Transmit Distortion on Tip/Ring



4.4 Trans-Hybrid Loss

As shown in Figure 4.4.A, the Audio Precision, AP1 injects a signal into the Tx inputs and measures the energy at Rx with Tip and Ring terminated by a 600Ω nominal impedance. The Tx input frequency is swept from 30Hz-4000Hz and the amplitude of the signal is measured on the Rx inputs and graphed in Figure 4.4.B.

Figure 4.4.A Trans-Hybrid Loss (THL) Test Setup

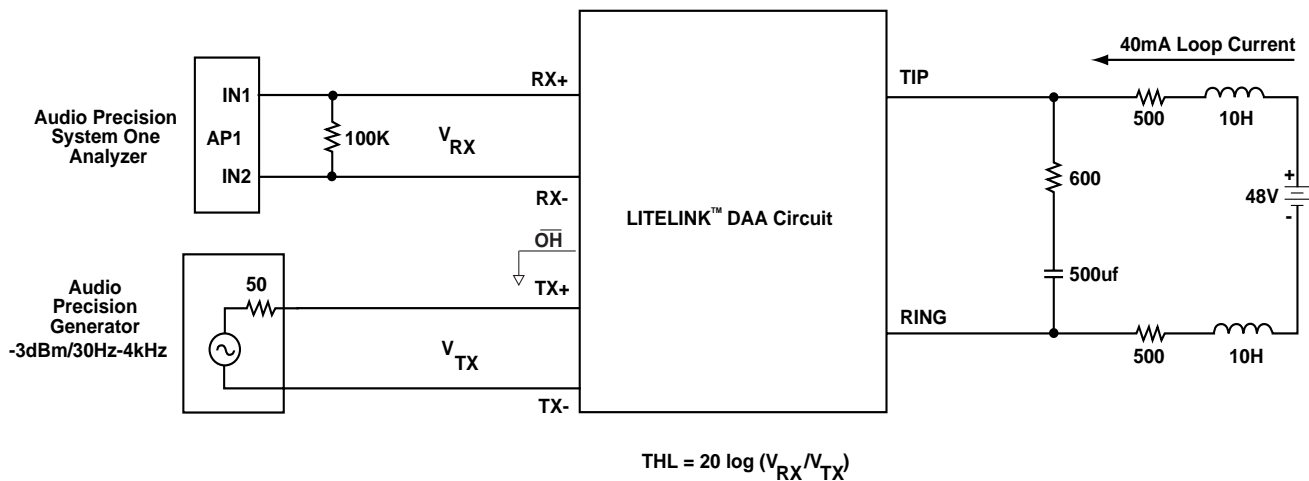
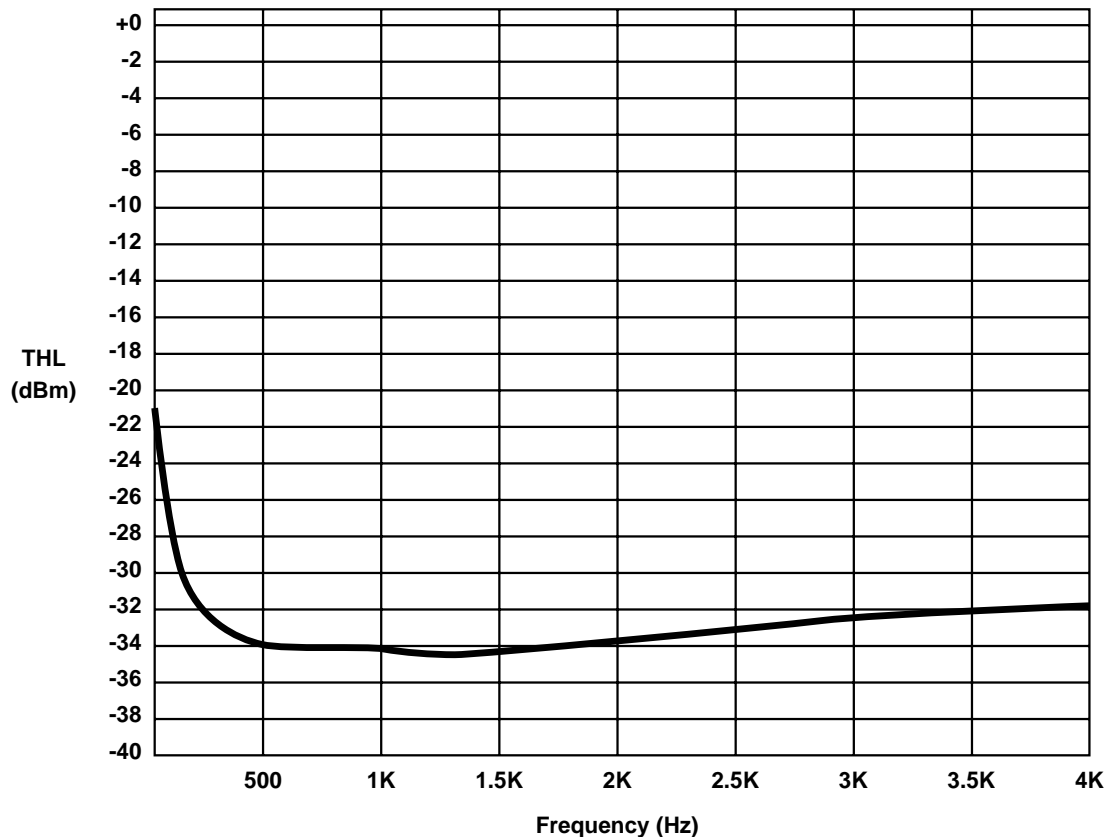


Figure 4.4.B Trans-Hybrid Loss at Rx± with -3dBm Signal on Tx± Matched to 600Ω Impedance on T/R



4.5 Return Loss

The return loss is a measure of impedance mismatch between a terminating impedance (DAA) and a source impedance (reference impedance). The AP measures the return loss vs. frequency with the addition of the bridge circuit show in Figure 4.5.A. For this test, the reference impedance is set by the 600Ω nominal impedance, Z_{REF} . The impedance that this is to be compared to is across Tip and Ring connections. The AP sweeps frequency and graphs frequency vs. return loss as shown in Figure 4.5.B.

Figure 4.5.A Return Loss Test Setup

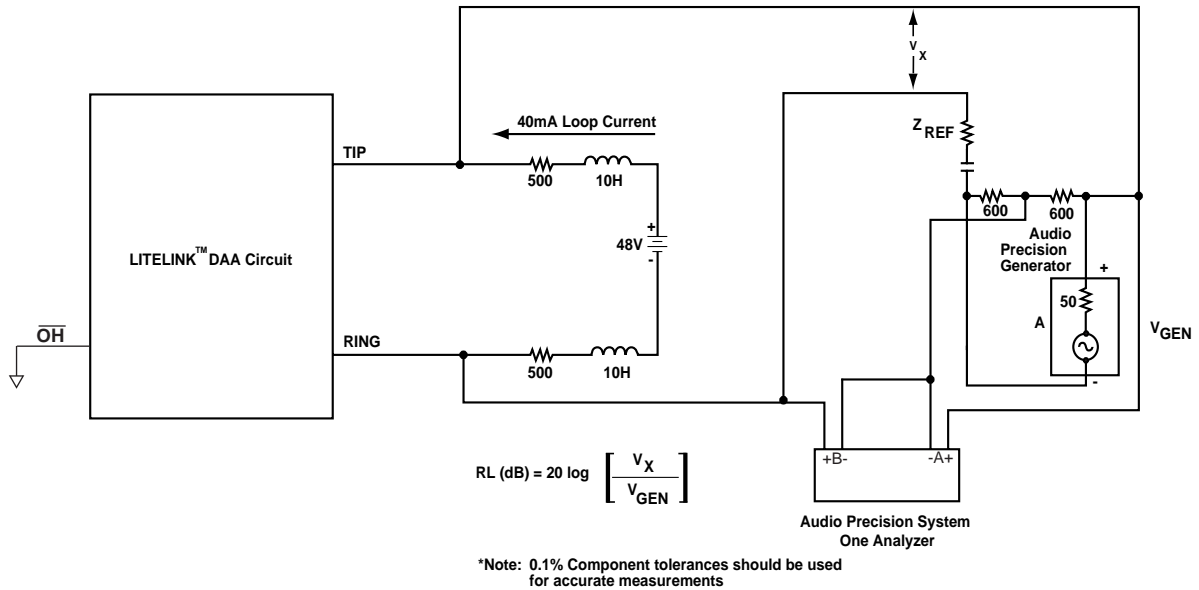
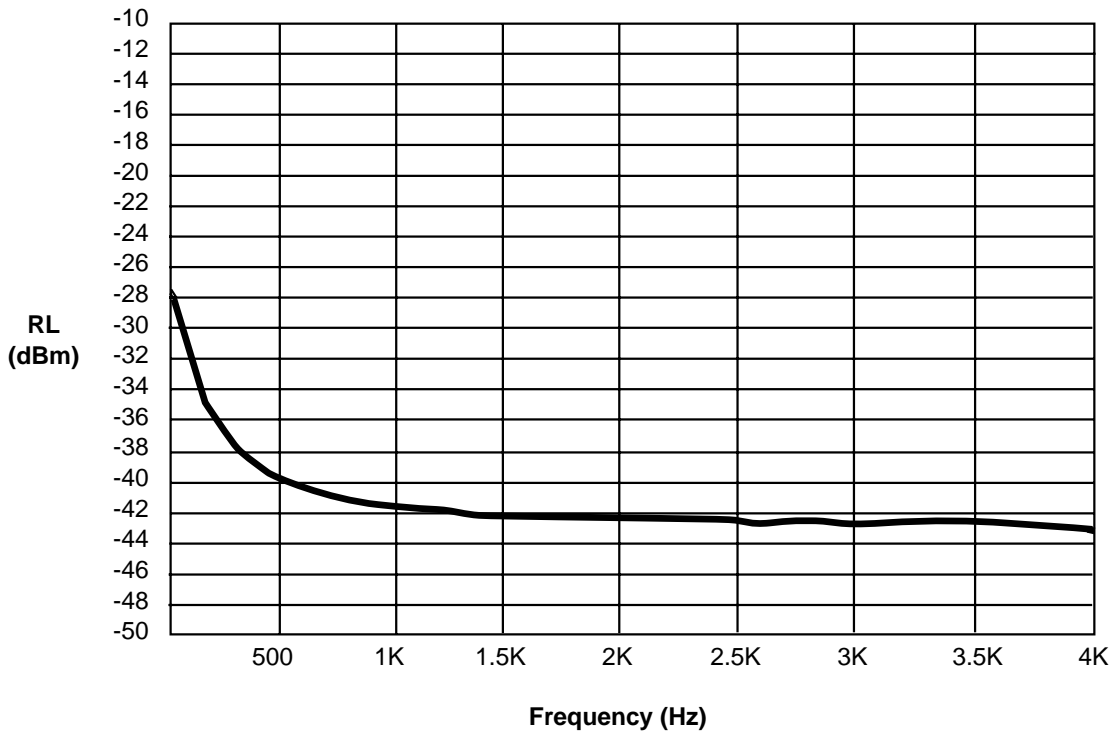


Figure 4.5.B Return Loss



4.6 Snoop Mode Frequency Response

Figure 4.6.A can be used as a reference test setup for this test with the difference being that the DAA is now in the on-hook mode. In the on-hook mode, the snoop circuit path is the signal path from Tip and Ring to Rx through the capacitive barrier C_S instead of the optical path. Snoop frequency response graph is shown in Figure 4.6.B.

Figure 4.6.A Snoop Mode Frequency Response Setup

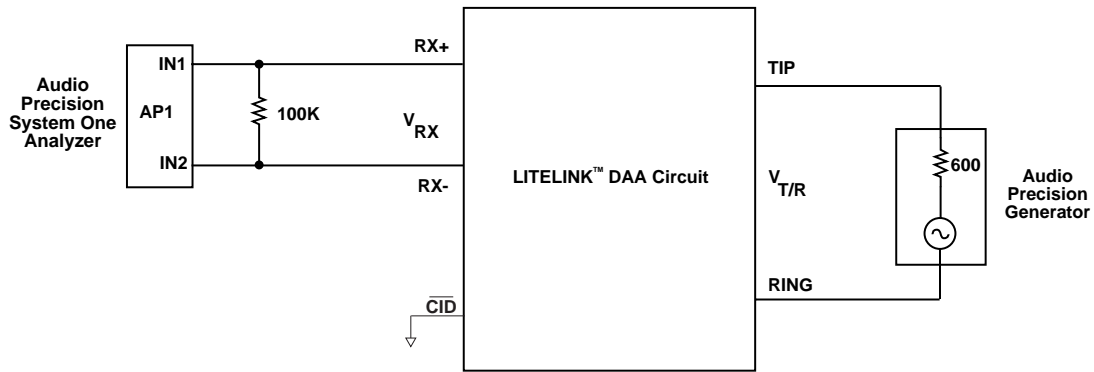
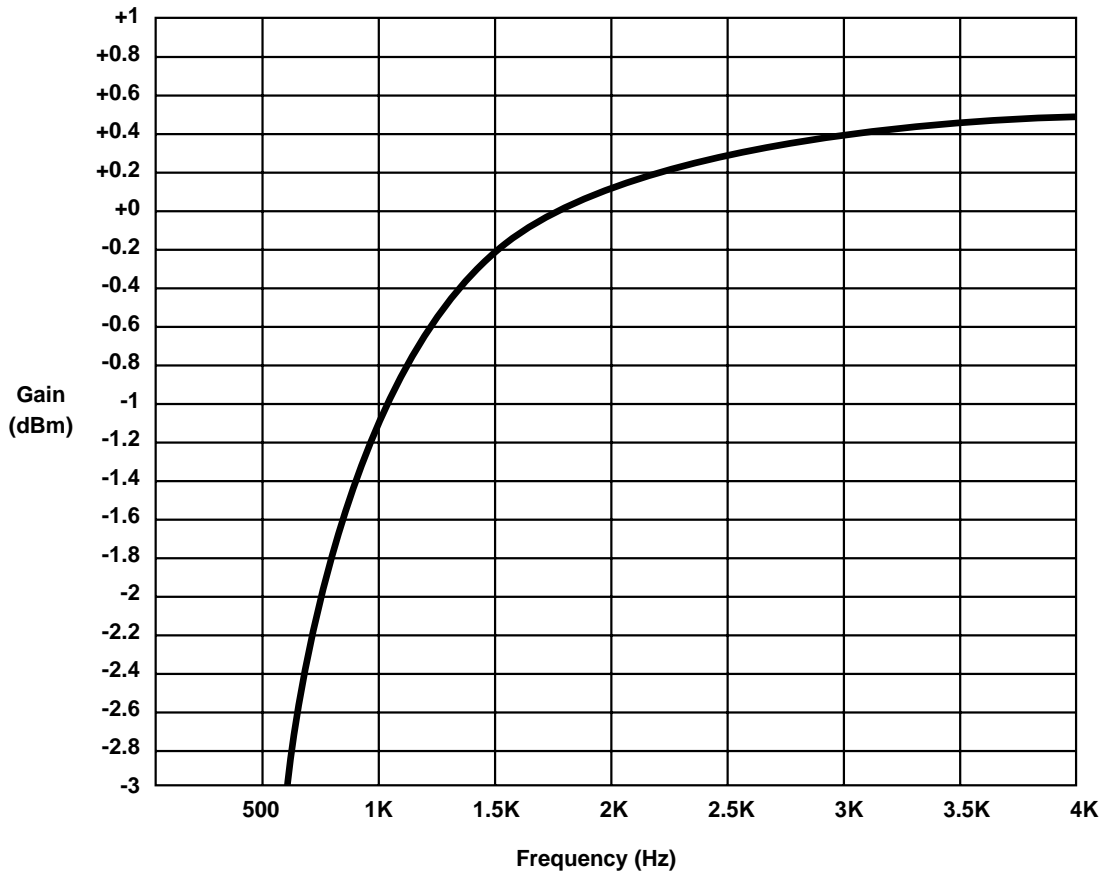


Figure 4.6.B Snoop Mode Frequency Response At Rx±



4.7 Snoop Mode Distortion

Figure 4.7.A can be used for the snoop mode distortion test. Snoop mode operation requires that the DAA be in the on-hook state and the $\overline{\text{CID}}$ pin asserted (driven Low). Distortion in the snoop mode is not critical since signals coupled through the snoop circuit are either 20Hz ring signals or FSK CID signals. A graph of THD+N for the snoop mode is shown in Figure 4.7.B.

Figure 4.7.A Snoop Mode Distortion Setup

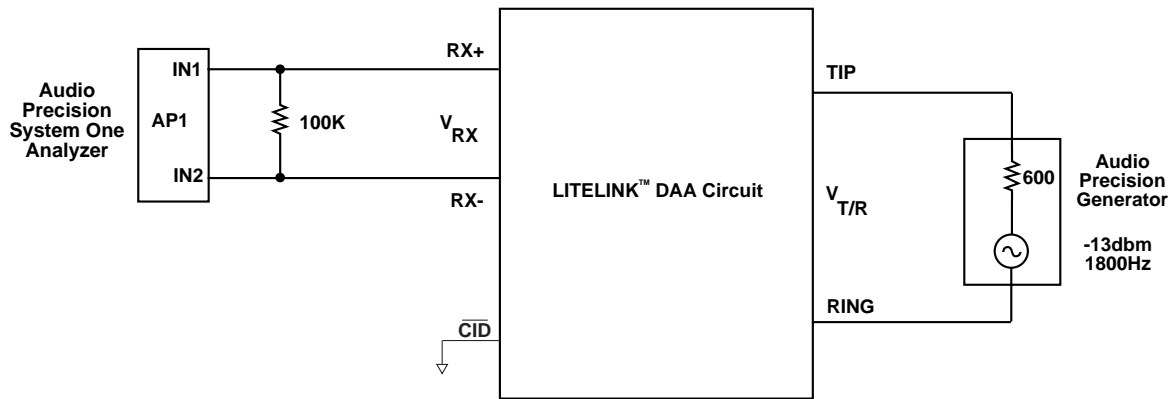
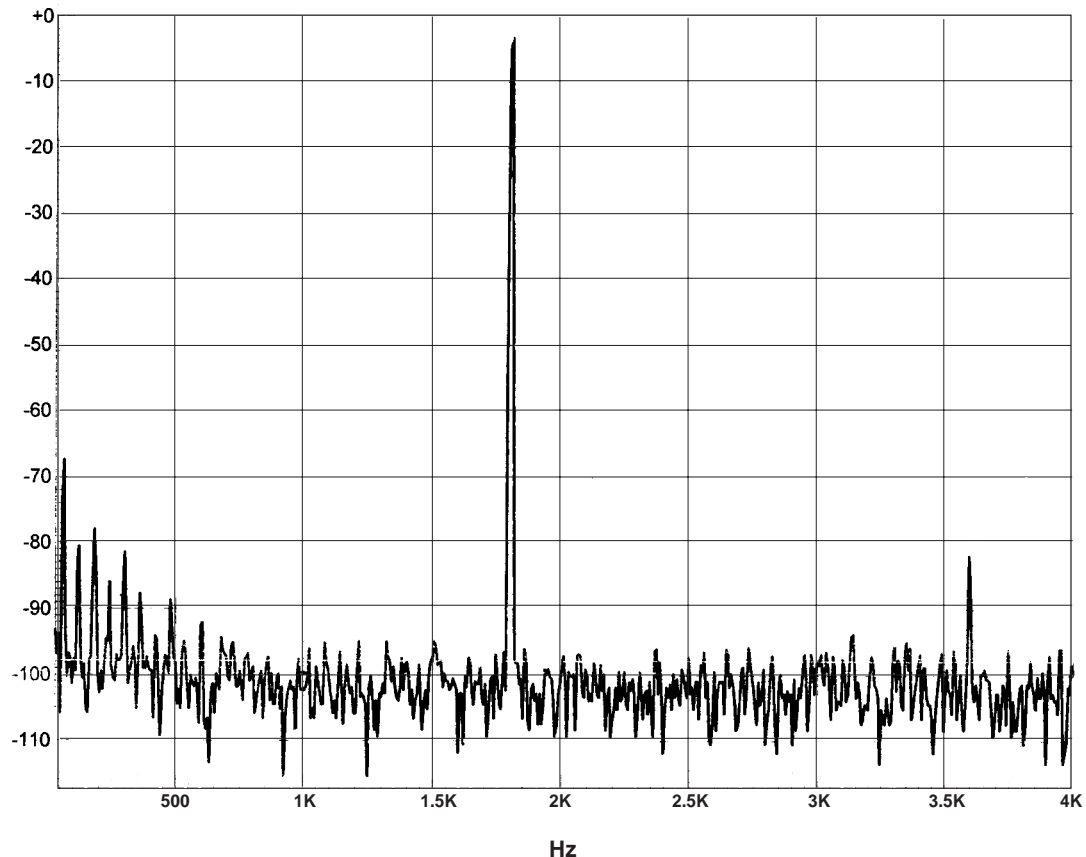


Figure 4.7.B Snoop Mode THD + N



4. 8 Snoop Mode Common Mode Rejection Ratio (CMRR)

As a practical matter, CMRR is dependent on how well the external snoop network C_S and R_{SNOOP} are matched. It is recommended that capacitors C_S (C6 or C7) be ceramic NPO (COG) type for excellent temperature stability and have a tolerance of 5% or less. Resistor tolerance for R_{SNOOP} (R5 or R6) should also be at least 5% or better.

Careful consideration should be taken related to PCB layout of the snoop network. Traces should be as short as possible and kept equidistant from one another. Spacing of 0.1" should be maintained between traces on the phone line side. If possible, traces should be routed away from large 60Hz fields to prevent noise inducement into the snoop circuit.

Figure 4.8.A shows the test setup for CMRR through the snoop signal path. For this test the LITELINK is on-hook and the frequency is swept from 20Hz to 4kHz. Figure 4.8.B is a graph of CMRR vs. frequency.

Figure 4.8.A Snoop Mode Common Mode Rejection Ratio Setup

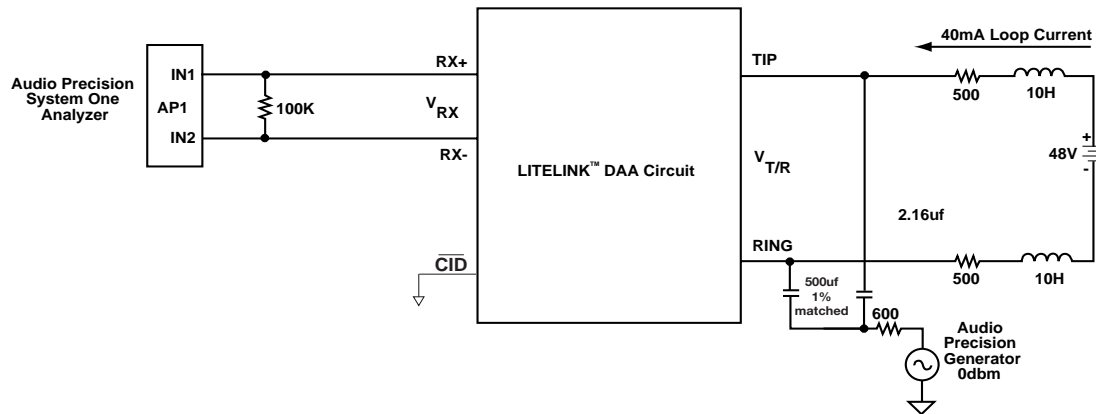
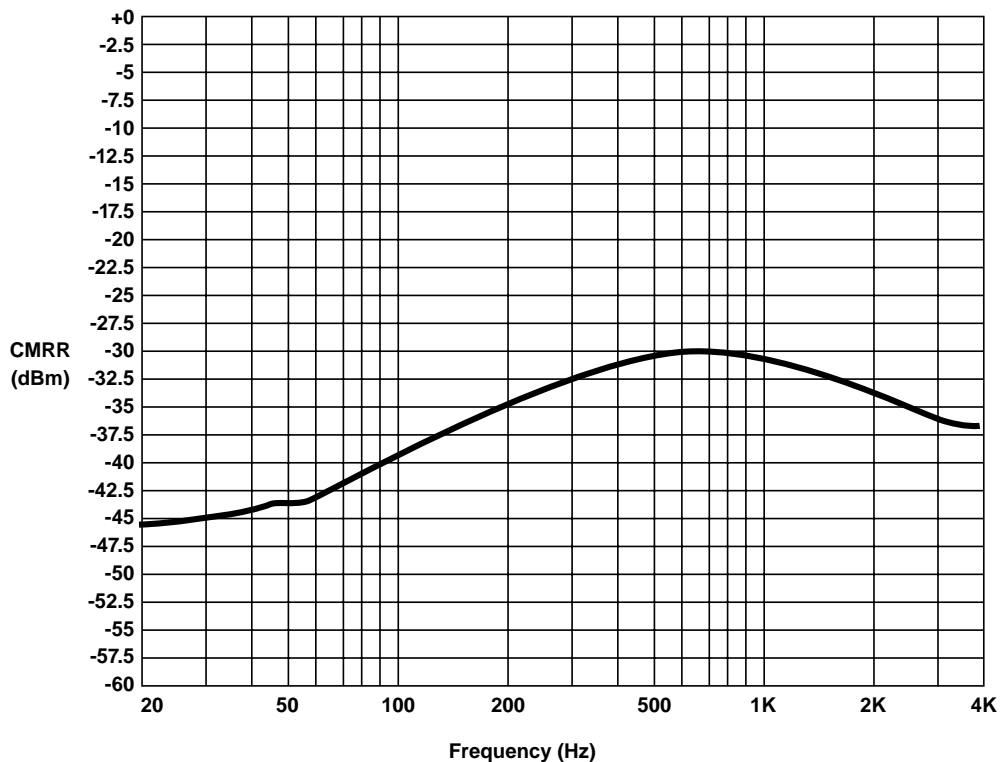
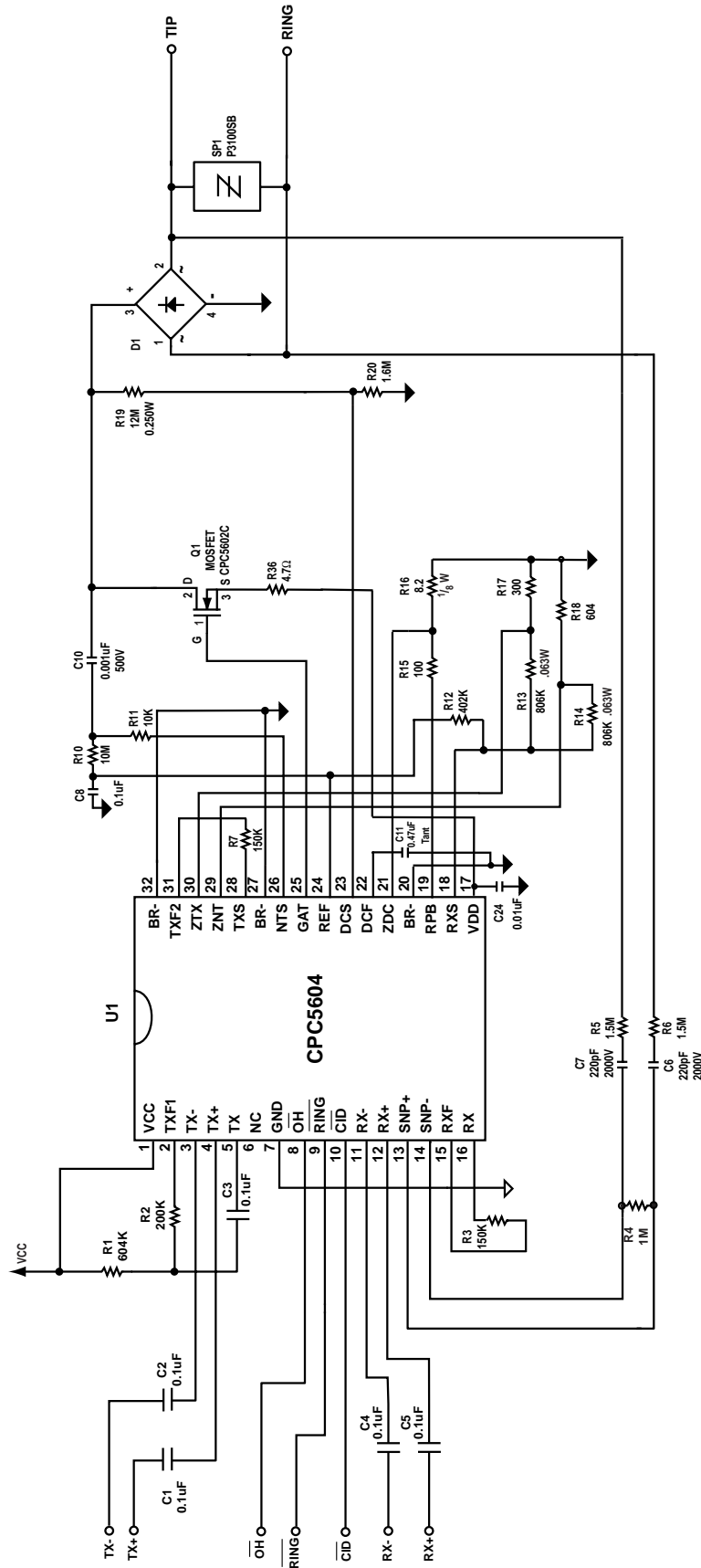


Figure 4.8.B Common Mode Rejection



5.0 APPLICATIONS

5.1 North American Reference Design Schematic



Drawn:	JCM/G	Date:	10/27/99	Rev:	B
Company:	CP Clare Corp.				
Title:	U.S. Reference Design				

ALL RESISTORS ARE 100W UNLESS OTHERWISE NOTED

5.2 North American Reference Design Bill of Materials

QTY.	Designation	Description	Manufacturer	Package Type
1	U1	CPC5604A	CP Clare	32 Lead SOIC
1	Q1	CPC5602C	CP Clare	SOT-223
1	R1	604k 1% Res.	Meritek	'0603
1	R18	604 ohm 1% Res.	Meritek	'0603
1	R2	200k 5% Res.	Meritek	'0603
1	R4	1M 5% Res	Meritek	0603
2	R3, R7	150k 5% Res.	Meritek	'0603
2	R5, R6	1.5M 5% Res.	Meritek	'1206
1	R11	10 K 5% Res.	Meritek	'0603
1	R12	402k 1% Res.	Meritek	'0603
1	R15	100 ohm 5% Res.	Meritek	'0603
2	R13, R14	806K 1% Res. 0.063W	Meritek	'0603
1	R16	8.2 5% Res. 1/8W	Meritek	'0603
1	R17	300 ohm 5% Res.	Meritek	'0603
1	R10	10M 5% Res.	Meritek	'0603
1	R19	12M 5% Res. 0.25W	Meritek	'1206
1	R20	1.6M 5% Res.	Meritek	'0805
1	R36	4.7 ohm 5% Res 1/8W	Meritek	'0603
5	C1, C2, C3, C4, C5	0.1 uf 50V 10% X7R	Tecate	'0805
2	C6, C7	220 pf 2000V NPO 5%	Tecate	1808
1	C8	0.1uf 50V 10% X7R	Tecate	'0805
1	C10	0.001uf 500V10% X7R	Tecate	1206
1	C11	0.47uf 25V Tant 10%	Panasonic	SMD
1	C24	.010 uf 50V 10% X7R	Tecate	0805
1	D1	Bridge Rectifier	Shindengen	N/A
1	SP1	Surge Protection	Teccor	D0-214AA
32	TOTAL			

5.4 International Reference Design Bill of Materials

QTY.	Designation	Description	Manufacturer	Package Type
1	U1	CPC5604A	CP Clare	32 Lead SOIC
1	U4	CPC5601D	CP Clare	S016
1	Q1	CPC5602C	CP Clare	SOT-223
1	R1	604k 1% Res.	Meritek	'0603
1	R18	604 ohm 1% Res.	Meritek	'0603
1	R2	200k 5% Res.	Meritek	'0603
1	R4	1M 5% Res.	Meritek	0603
2	R3, R7	150k 5% Res.	Meritek	'0603
2	R5, R6	1.5M 5% Res.	Meritek	'1206
2	R11, R21	10 K 5% Res.	Meritek	'0603
1	R12	402k 1% Res.	Meritek	'0603
1	R15	100 ohm 5% Res.	Meritek	'0603
2	R13, R14	806K 1% Res. 0.063W	Meritek	'0603
1	R16	22.1 1% Res. 1/8W	Meritek	'0603
1	R17	300 ohm 5% Res.	Meritek	'0603
1	R10	10M 5% Res.	Meritek	'0603
1	R19	12M 5% Res. 0.25W	Meritek	'1206
1	R20	1.6M 5% Res.	Meritek	'0805
1	R23	470 ohm 5% Res.	Meritek	'0603
1	R24	8.2k 5% Res. 0.25W	Meritek	'0603
5	R22, R29, R30, R31, R32	Open	-	'0603
1	R25	590 ohm 5% Res.	Meritek	'0603
1	R26	0 ohm Res.	Meritek	'0603
1	R27	0 ohm Res.	Meritek	'0603
1	R28	Open	-	'0603
1	R33	12.1 ohm 1% Res.	Meritek	'0603
1	R34	0 ohm 5% Res.	Meritek	'0603
1	R36	4.7 ohm 5% Res 1/8W	Meritek	'0603
5	C1, C2, C3, C4, C5	0.1 uf 50V 10% X7R	Tecate	'0805
2	C6, C7	220 pf 2000V NPO 5%	Tecate	1808
1	C8	0.1uf 50V 10% X7R	Tecate	'0805
1	C10	0.001uf 500V10% X7R	Tecate	1206
1	C11	0.47uf 25V Tant 10%	Panasonic	SMD
1	C14	.47uf 300V	Tecate	1812
1	C15	Open	-	'0805
1	C16	0.0047uf 50V 10% X7R	Tecate	'0805
1	C17	Open for future use	-	'0805
1	C24	0.01uf 50V 10% X7R	Tecate	0805
1	SP1	Surge Protection	Teccor	D0-214AA
2	Z1, Z2	Zener 20V	Rohm	SOT-23
1	D1	Bridge Rectifier	Shindengen	N/A
1	D2	Diode BAS16	Rohm	SOT-23
53	TOTAL			

5.6 CTR-21 Reference Design Bill of Materials

QTY.	Designation	Description	Manufacturer	Package Type
1	U1	CPC5604A	CP Clare	32 Lead SOIC
1	Q1	CPC5602C	CP Clare	SOT-223
1	R1	604k 1% Res.	Meritek	'0603
1	R4	1M 5% Res.	Meritek	0603
1	R18	604 ohms 1% Res.	Meritek	'0603
1	R2	200k 5% Res.	Meritek	'0603
2	R3, R7	150k 5% Res.	Meritek	'0603
2	R5, R6	1.5M 5% Res.	Meritek	'1206
1	R11	10 K 5% Res.	Meritek	'0603
1	R12	402k 1% Res.	Meritek	'0603
1	R15	100 ohm 5% Res.	Meritek	'0603
2	R13, R14	806K 1% Res. 0.063W	Meritek	'0603
1	R16	22.1 5% Res. 1/8W	Meritek	'0603
1	R17	300 ohm 5% Res.	Meritek	'0603
1	R10	10M 5% Res.	Meritek	'0603
1	R19	12M 5% Res. .25W	Meritek	'1206
1	R20	1.6M 5% Res.	Meritek	'0805
1	R21	12.1 5% Res. 0.063W	Meritek	'0603
1	R36	4.7 ohm 5% Res 1/8 W	Meritek	'0603
5	C1, C2, C3, C4, C5	0.1 uf 50V 10% X7R	Tecate	'0805
2	C6, C7	220 pf 2000V NPO 5%	Tecate	1808
1	C8	0.1uf 50V 10% X7R	Tecate	'0805
1	C10	0.001uf 500V10% X7R	Tecate	1206
1	C11	0.47uf 25V Tant 10%	Panasonic	SMD
1	C24	0.01uf 50V 10% X7R	Tecate	'0805
1	C25	0.0047uF 50V 10% X7R	Tecate	'0805
1	D1	Bridge Rectifier	Shindengen	N/A
1	SP1	Surge Protection	Teccor	D0-214AA
1	U2	4N35		
35	TOTAL			

5.8 CTR-21 with Exceptions Reference Design Bill of Materials

QTY.	Designation	Description	Manufacturer	Package Type
1	U1	CPC5604A	CP Clare	32 Lead SOIC
1	Q1	CPC5602C	CP Clare	SOT-223
1	R1	604k 1% Res.	Meritek	'0603
1	R18	604 ohm 1% Res.	Meritek	'0603
1	R2	200k 5% Res.	Meritek	'0603
1	R4	1M 5% Res	Meritek	0603
2	R3, R7	150k 5% Res.	Meritek	'0603
2	R5, R6	1.5M 5% Res.	Meritek	'1206
1	R11	10 K 5% Res.	Meritek	'0603
1	R12	402k 1% Res.	Meritek	'0603
1	R15	100 ohm 5% Res.	Meritek	'0603
2	R13, R14	806K 1% Res. 0.063W	Meritek	'0603
1	R16	22.1 1% Res. 1/8W	Meritek	'0603
1	R17	300 ohm 5% Res.	Meritek	'0603
1	R10	10M 5% Res.	Meritek	'0603
1	R19	12M 5% Res. 0.25W	Meritek	'1206
1	R20	1.6M 5% Res.	Meritek	'0805
1	R21	12.1 1% Res. 0.063W	Meritek	'0603
1	R22	0 ohm	Meritek	'0603
1	R35	Open	-	'0603
1	R36	4.7 ohm 5% Res 1/8 W	Meritek	'0603
5	C1, C2, C3, C4, C5	0.1 uf 50V 10% X7R	Tecate	'0805
2	C6, C7	220 pf 2000V NPO 5%	Tecate	1808
1	C8	0.1uf 50V 10% X7R	Tecate	'0805
1	C10	0.001uf 500V10% X7R	Tecate	1206
1	C11	0.47uf 25V Tant 10%	Panasonic	SMD
1	C18	0.0047uF 50V 10% X7R	Tecate	'0805
1	C24	0.01uf 50V 10% X7R	Tecate	0805
1	D1	Bridge Rectifier	Shindengen	N/A
1	SP1	Surge Protection	Teccor	D0-214AA
1	U2	4N35		
1	U3	4N35		
1	U5	4N35		
39	TOTAL			

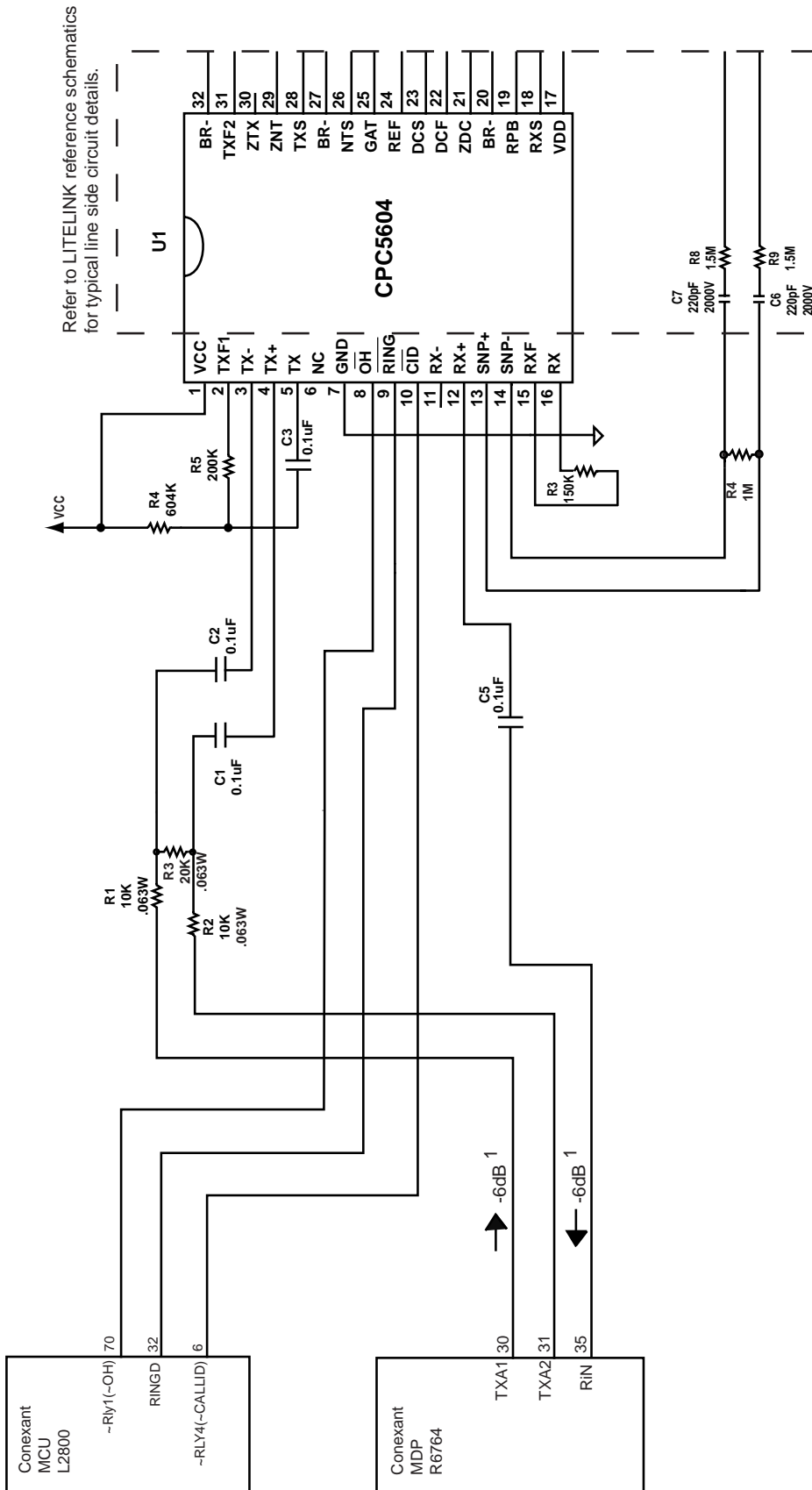
5.9 Country Specific Component Values

	RZDC	ZZNT
US	8.2Ω	600Ω
CTR-21	22.1Ω	600Ω 0.0047μF
Far East	8.2Ω	600Ω

CTR-21 Countries:

UK
 Canada
 France
 Germany
 Spain
 Switzerland
 Italy
 Luxembourg
 Holland
 Belgium
 Netherlands
 Australia
 Japan

5.10 Interconnection to Rockwell 56k Chipset

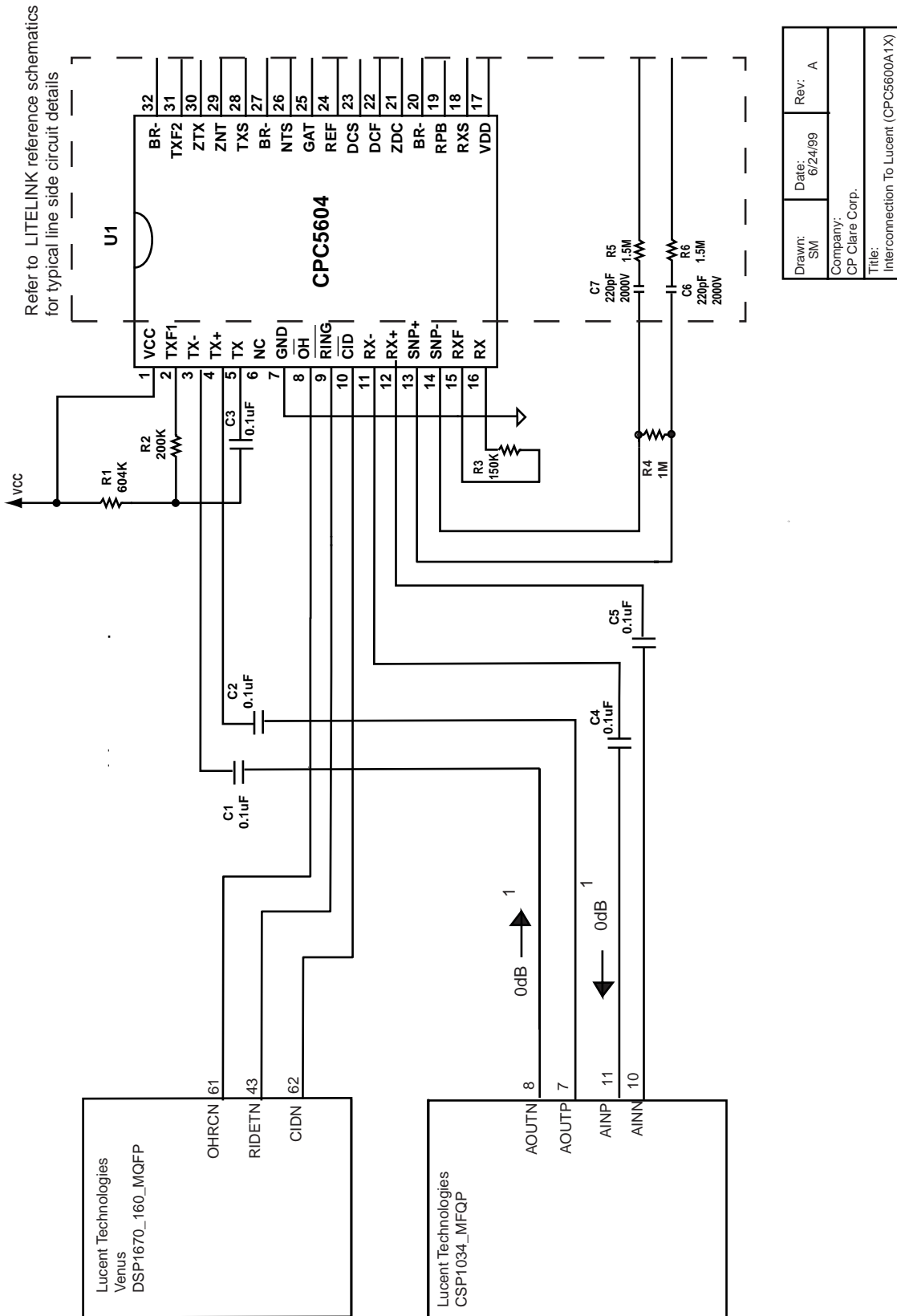


Drawn: SM	Date: 6/24/99	Rev: A
Company: C.P.Clare Corp.		
Title: Interconnection to Conexant(Rockwell) (CPC5600A1X)		

ALL RESISTORS ARE .100W
UNLESS OTHERWISE NOTED

Interconnection diagram is based on the Conexant(Rockwell) RC56D Chip solution.
1. Conexant Chipsets rely on a 6dB loss between MDP and tip and ring. This is solved by placing the R1, R2, R3, resistor circuit in the Transmit Path and the use of a single end of the differential receive.

5.11 Interconnection to Lucent 56k Chipset



1. Lucent chips expect a zero dB drop between the codec and Tip and Ring.

ALL RESISTORS ARE .100W UNLESS OTHERWISE NOTED

NORTH AMERICA**North American Sales Office**

CP Clare Corporation
78 Cherry Hill Drive
Beverly, MA 01915
Tel: 1-978-524-6700
Fax: 1-978-524-4900
Toll Free: 1-800-CPCLARE

Eastern Regional Sales

CP Clare Corporation
78 Cherry Hill Drive
Beverly, MA 01915
Tel: 1-978-524-6700
Fax: 1-978-524-4900
Toll Free: 1-800-CPCLARE

Mid-American Regional Sales

CP Clare Corporation
78 Cherry Hill Drive
Beverly, MA 01915
Tel: 1-978-524-6700
Fax: 1-978-524-4900
Toll Free: 1-800-CPCLARE

Northwestern Regional Sales

CP Clare Corporation
2010 Crow Canyon Place
Suite 100
San Ramon, CA 94583
Tel: 1-925-277-3422
Fax: 1-925-277-3423
Toll Free: 1-800-CPCLARE

Southwestern Regional Sales

CP Clare Corporation
2816 Nevis Circle
Costa Mesa, CA 92626
Tel: 1-714-556-3661
Fax: 1-714-546-4254
Toll Free: 1-800-CPCLARE

Canadian Regional Sales

Clare Canada Ltd.
3425 Harvester Road
Suite 202
Burlington, Ontario L7N 3N1
Tel: 1-905-333-9066
Fax: 1-905-333-1824

EUROPE**European Sales Office**

CP Clare nv
Bampsiaan 17
B-3500 Hasselt (Belgium)
Tel: 32-11-300868
Fax: 32-11-300890

France

CP Clare France
31 Cours des Juilliottes
94700 Maisons Alfort
France
Tel: 33 (1) 56-29-14-14
Fax: 33 (1) 56-29-14-15

Germany

CP Clare Elektronik GmbH
Leonberger Strasse 20
D-71638, Ludwigsburg
Tel: 49-7141-9543-0
Fax: 49-7141-9543-20

Italy

C.L.A.R.E.s.a.s.
Via C. Colombo 10/A
I-20066 Melzo (Milano)
Tel: 39-02-95737160
Fax: 39-02-95738829

Sweden

Clare Sales
Comptronic AB
Box 167
S-16329 Spånga
Tel: 46-862-10370
Fax: 46-862-10371

United Kingdom

Clare UK Sales
Marco Polo House
Cook Way
Bindon Road
Taunton
UK-Somerset TA2 6BG
Tel: 44-1-823 352541
Fax: 44-1-823 352797

ASIA PACIFIC**Asian Sales Office**

CP Clare Corporation
Room N1016, Chia-Hsin, Bldg
II,
10F, No. 96, Sec. 2
Chung Shan North Road
Taipei, Taiwan R.O.C.
Tel: 886-2-2523-6368
Fax: 886-2-2523-6369

JAPAN**Japanese Sales Office**

CP Clare Corporation
Tosei Building 5F
2-23-1, Ikebukuro, Toshima-ku
Tokyo 171
Tel: 03-3980-2212
Fax: 03-3980-2213

HEADQUARTERS

CP Clare Corporation
78 Cherry Hill Drive
Beverly, MA 01915
Tel: 1-978-524-6700
Fax: 1-978-524-4900
Toll Free: 1-800-CPCLARE

<http://www.cpclare.com>

CP Clare Corporation makes no assertion or warranty that the circuitry and the uses thereof disclosed herein are non-infringing on any valid US or foreign patents. CP Clare assumes no liability as a result of the use of said specifications and reserves the right to make changes to specifications without notice. CP Clare does not authorize or warrant any CP Clare device for use in life support devices and/or systems. Contact your nearest CP Clare Sales Office for the latest specifications.

Protected by U.S. Patent #5,946,394

Specifications: AN-LITELINK-CPC5604-R2
©Copyright 2000, CP Clare Corporation
All rights reserved. Printed in USA.
1/27/00