

XMEGA

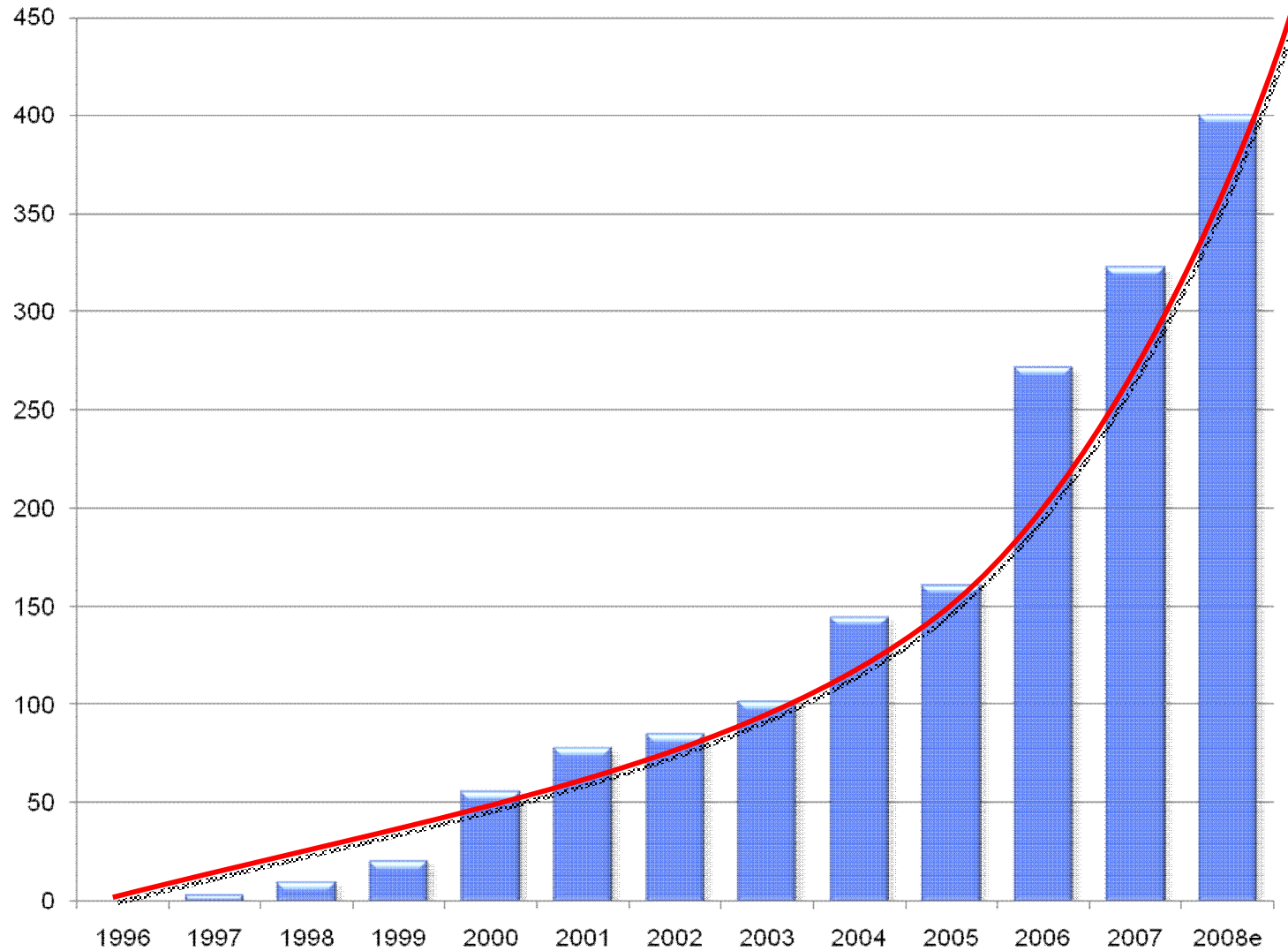
ARGUSSOFT

AVR[®] XMEGA[™]

A New Reference for 8/16-bit Microcontrollers



AVR revenue growth



AVR

Success Through Innovation

n Atmel

- § **First Flash MCU**
- § **First MCU with In-System Programmable Flash and EEPROM**

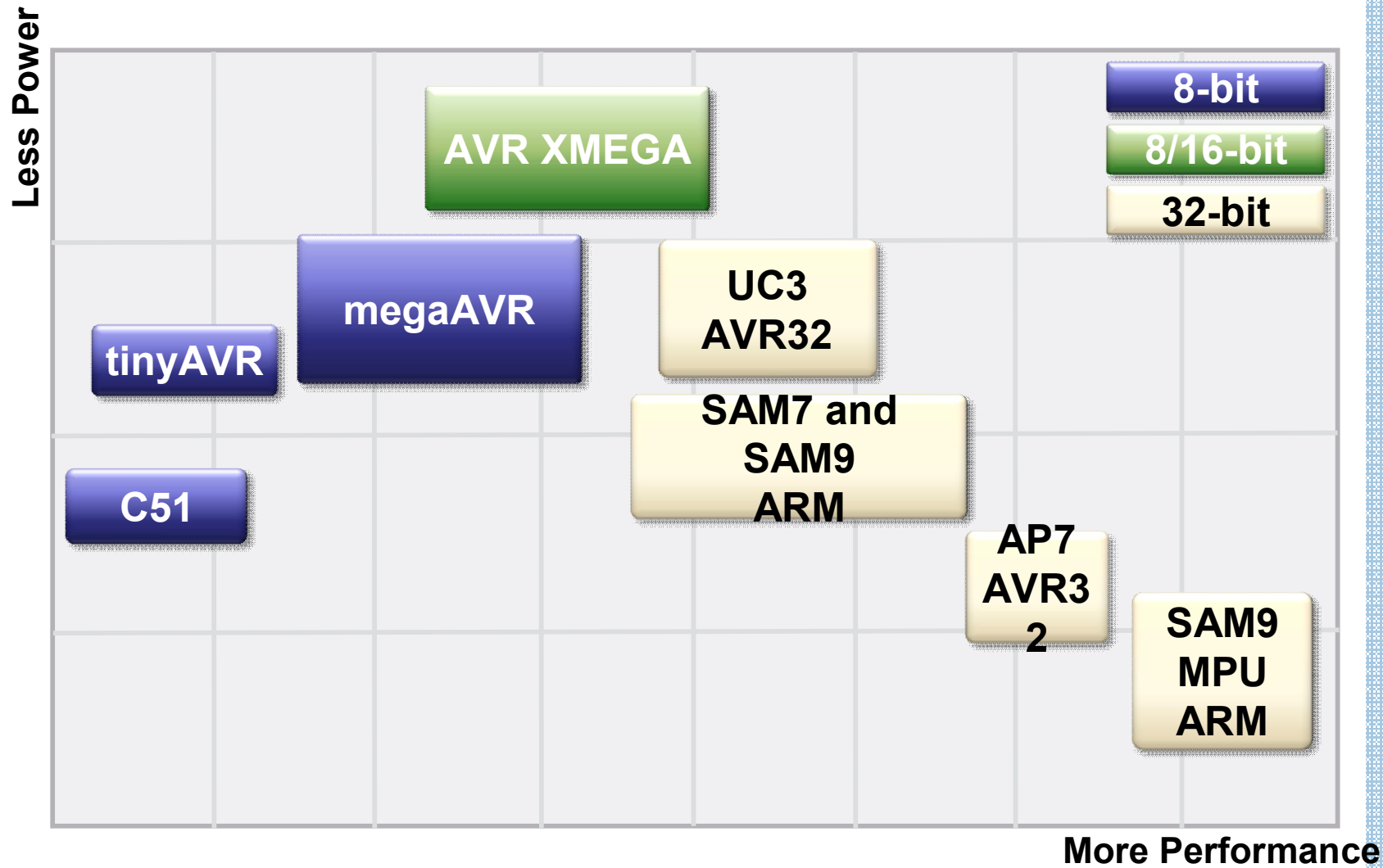
n AVR

- § **First and only 8-bit designed for C**
- § **First with true 1.8V operation**
- § **First with 100nA power down operation**
- § **First true low power management system and technology – picoPower**

n AVR Development Tools

- § **First full-featured IDE free of charge – AVR Studio**
- § **First sub \$50 general debugger – AVR Dragon**
- § **First free IDE with open plug-in interface – AVR Studio**

Atmel's MCU Product offering



More Performance



Next generation AVR

n Atmel is dedicated to 8/16-bit market

n **Extraordinary Low Power**

- § 2nd generation picoPower®

- § True 1.6 V operation

n **Exceptional Performance**

- § Up to 32 MIPS

- § DMA Controller

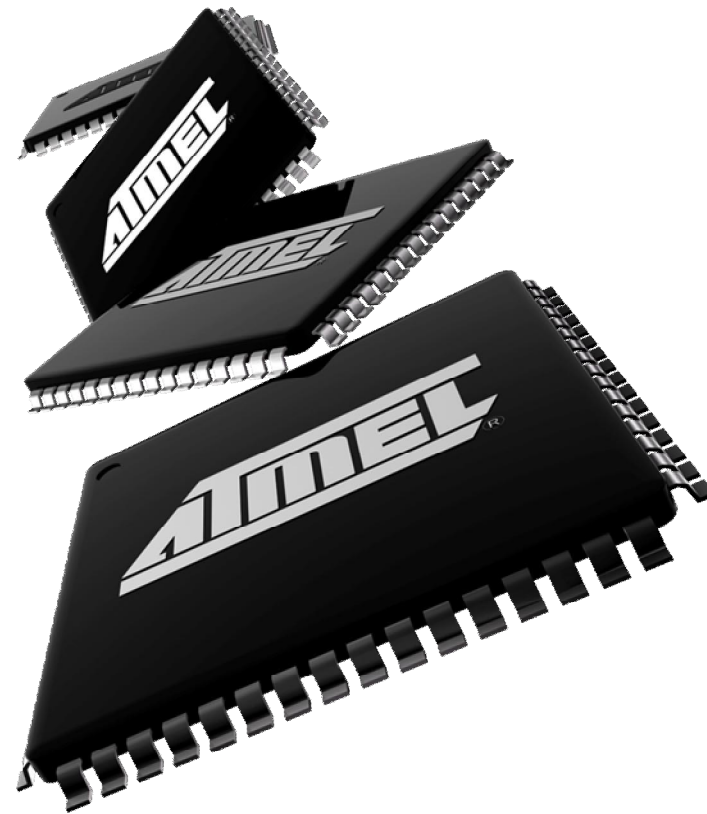
- § Event System

n **Extreme Peripherals**

- § Leading Analog Integration

- § Fast Crypto engine

- § Rich feature set



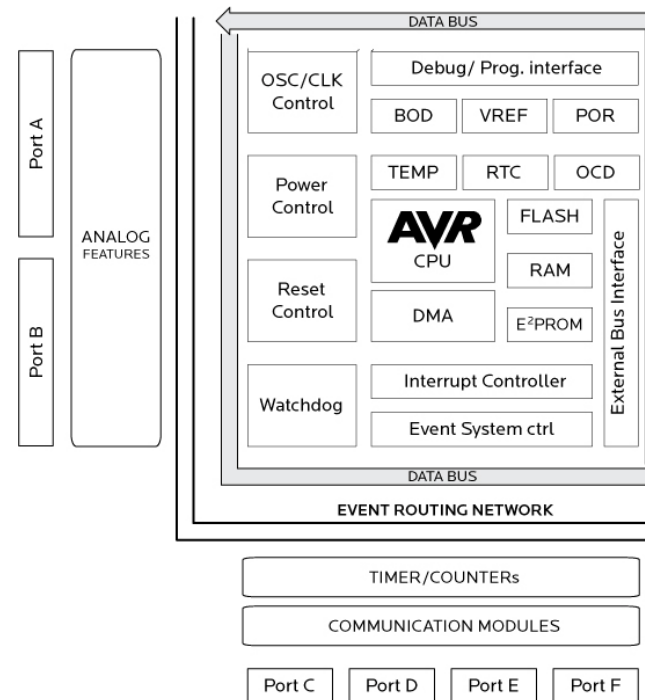
2nd generation picoPower

- n Industry leading in low power applications
- n True 1.6V operation
 - § Flash, Analog, EEPROM, Oscillators down to 1.6V
 - § VCC = 1.8V +/-10%
- n Lowest power 32 kHz Crystal Oscillator
 - § 650nA RTC
- n Low leakage Process Technology
 - § 100nA
- n 1 μ A Watchdog and Brown-Out



XMEGA Event system

- n Inter-peripheral communication**
 - § CPU and DMA independent
- n Latency free event handling**
 - § Safe fault protection
 - § 100% predictable reaction time
- n Reduces power consumption**
- n 8 parallel channels**



Leading Analog Features

n 2 Msps 12-bit ADC

- § Hardware support for ADC oversampling (16-bit)
- § Programmable gain stage removes external gain

n 1 Msps 12-bit DAC

n 10 mA output drives

n High EMC performance

- § Reduced need for external protection

n $\pm 1\%$ Internal Oscillators

- § Communication can run from internal RC

XMEGA Crypto engine

n Supports up to 1.25 Mbps AES encrypted communication

n AES

§ 128-bit key length

§ Encryption of 16 bytes in 375 clock cycles

§ Decryption of 16 bytes in 375 clock cycles

n DES

§ 56-bit key length

§ Encryption of 8 bytes in 16 clock cycles

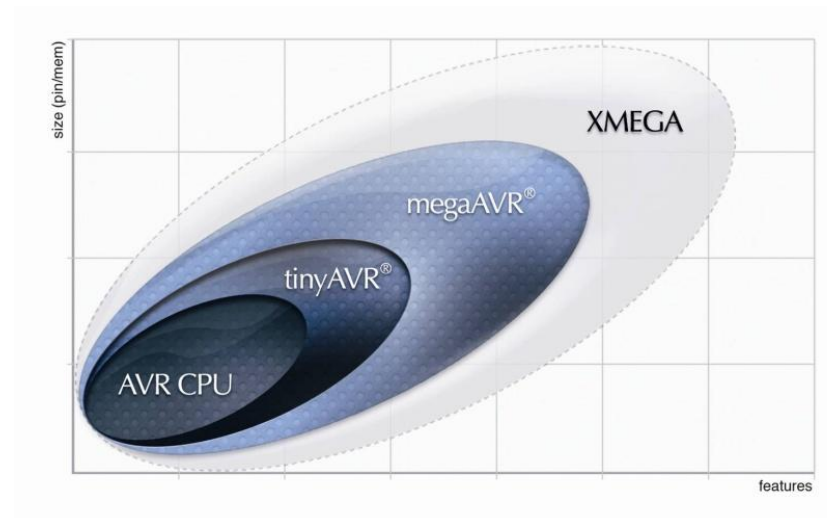
§ Decryption of 8 bytes in 16 clock cycles

```
Sosokokatototeno  
n0error0gogojjem  
omotot0unonodode  
ror0XoX
```



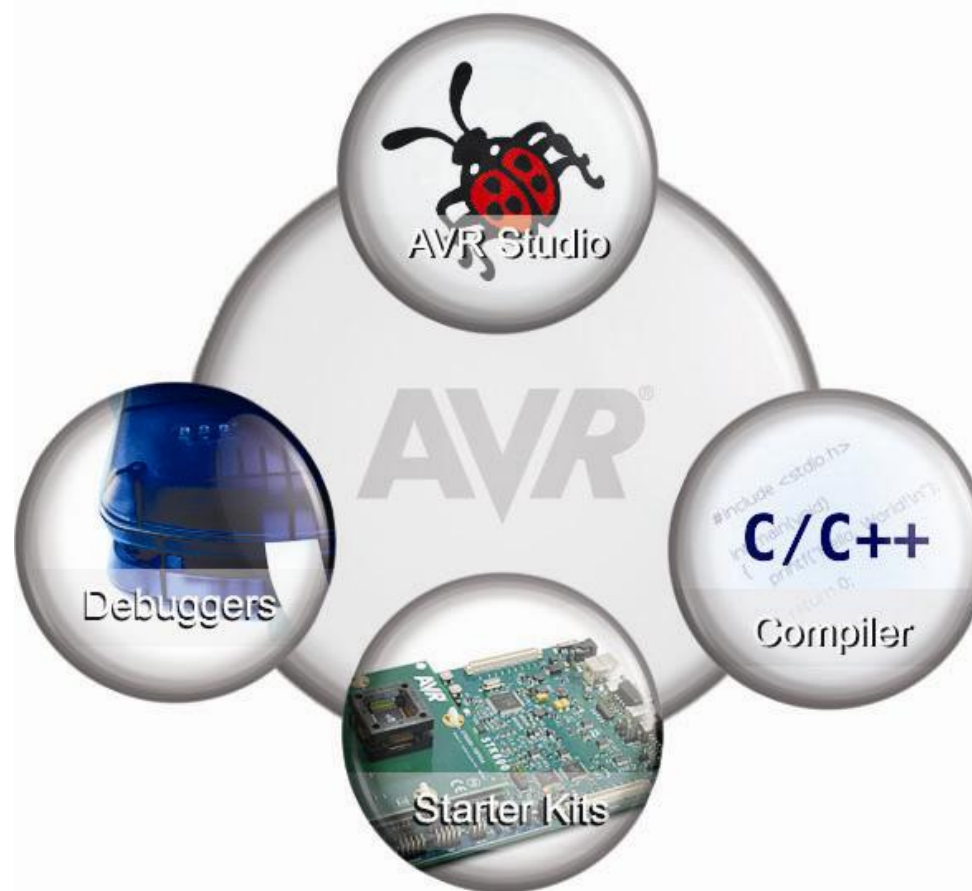
Compatibility and Migration

- n Same CPU as megaAVR and tinyAVR
 - § Reuse existing code
 - § Reuse existing development tools
- n AVR covers entire 8/16 bit market
- n All XMEGA are hex-compatible
 - § Develop with ATxmega128A1
 - § Device selection at later stage



Easy to use tool-chain

- n Free AVR Studio
- n Free AVR GCC compiler
- n JTAG ICE mkII debugger
- n STK600 development kit



STK600 Development Kit



XMEGA Technical walk-through

XMEGA AVR CPU

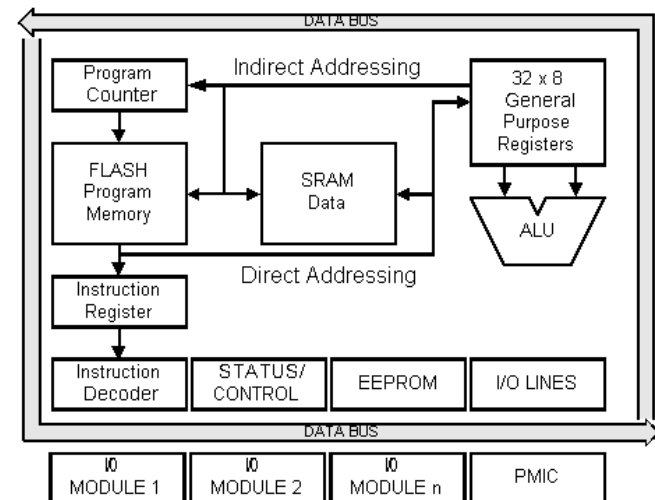
n Code compatible with existing tinyAVR and megaAVR

- § True RISC architecture
- § True single cycle execution
- § 32 MIPS at 32 MHz
 - 32 MHz 2.7V – 3.6V 12 MHz 1.8V – 2.7V
- § 32 General Purpose registers
- § Harvard architecture

n Adds DMA Controller

n Adds flexible Event System

n Adds Programmable Multi level Interrupt Controller



XMEGA DMA Controller

n Allows high-speed data transfer

- § From memory to peripheral
- § From memory to memory
- § From peripheral to memory
- § From peripheral to peripheral

n Main features

- § 4 channels
- § Up to 64kb transfers
- § Optional interrupt at end of transmission
- § Multiple addressing modes
 - Static, Increment, Decrement
- § Cycle stealing and burst modes
- § Programmable priority between channels

XMEGA Interrupt Controller

n 4 level of interrupts

§ NMI - Non Maskable Interrupts

- Can be enabled, but not disabled by SW
- Crystal Oscillator stop detection

§ High, Medium and Low level

- Medium level will interrupt even when low level interrupt service routines are running

n User selectable enable / disable of interrupts

n User selectable interrupt level for each interrupts source

n Round robin priority possible for low level interrupts

§ Ensures all interrupts are serviced

n All peripherals can also be controlled by polling

XMEGA Event system

n Advanced routing system for autonomous control of peripherals

n 8 Event Routing Channels

n Peripherals specify how to generate events

§ In general everything that can generate an interrupt

§ Ex: Pin change, Timer overflow, ADC complete, Comparator toggle

n Peripherals specify how to use events

§ Ex: Increment Timer, Output signal, Start ADC conversion

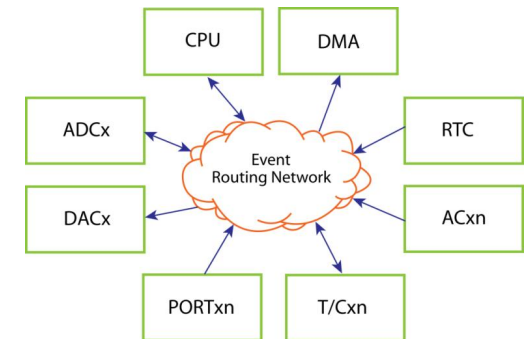
n Event system is signal routing only

§ Extremely powerful since it will reduce the use of interrupts

§ Event system ensures control of critical functions

- Predictable reaction time – 2 chip clock cycles (100 ns @ 20 MHz)
- Reliable between SW revisions

n Event system active in Active and Idle mode



XMEGA memories

n Flash

- § Application area for main program
- § Boot area for bootloader
- § Application Table area for fail safe EEPROM emulation

n EEPROM

- § EEPROM on all devices
- § Byte and page accessible
- § Optional memory mapped

n SRAM

- § Internal on all devices
- § Optional external on some devices
 - Up to 16 MB directly addressable
 - Optional multiplexed address and data

n Memory setup

Flash	SRAM	EEPROM
16K + 4K	2K	1K
32K + 4K	4K	1K
64K + 4K	4K	1K
128K + 8K	8K	2K
256K + 8K	16K	4K

n SDRAM

- § Optional external on some devices
 - Up to 128 Mbit directly addressable
 - 4-bit and 8-bit supported

XMEGA Analog to Digital Converter

n Features

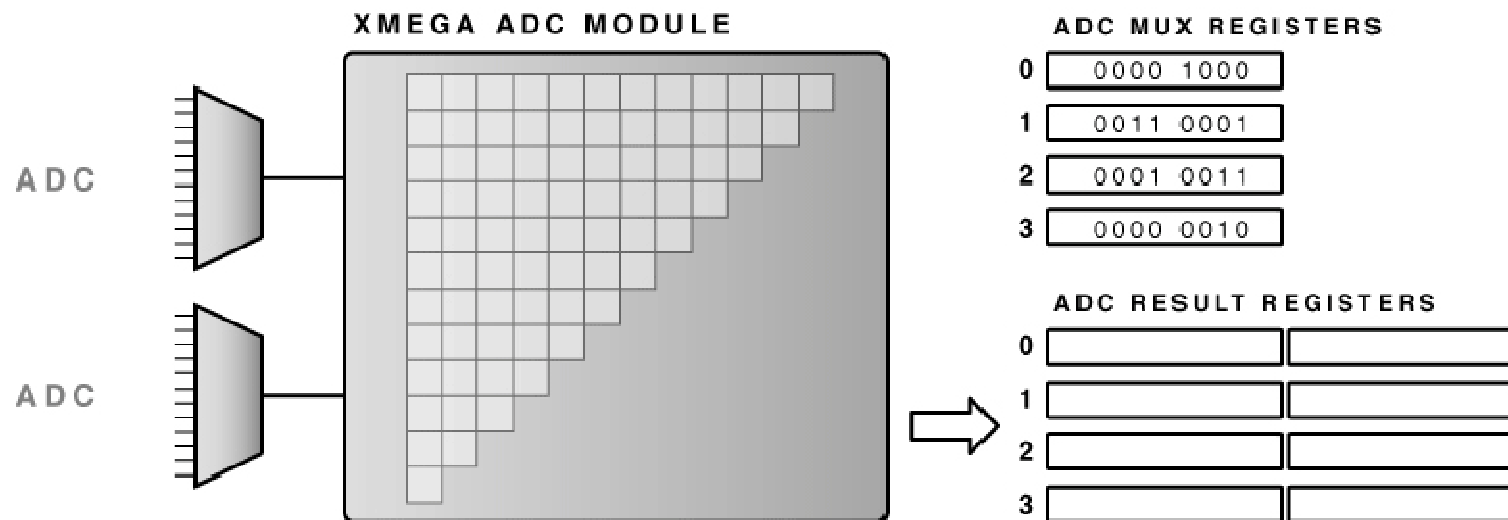
- § 12 bit, 2Msps ADC
- § Single or continuous conversion modes
- § 8 or 12 bits accuracy SW selectable
 - 8 bit result has 2.5 us propagation delay
 - 12 bit result has 3.5 us propagation delay
- § Connected to Event System
- § Connected to DMA Controller
- § Built-in gain calibration
- § Internal and External reference voltages

n Interrupt/event on compare result

- § Interrupt if lower or equal
- § Interrupt if higher or equal

n Interrupt/event on conversion complete

XMEGA ADC – pipelining 4 virtual channels

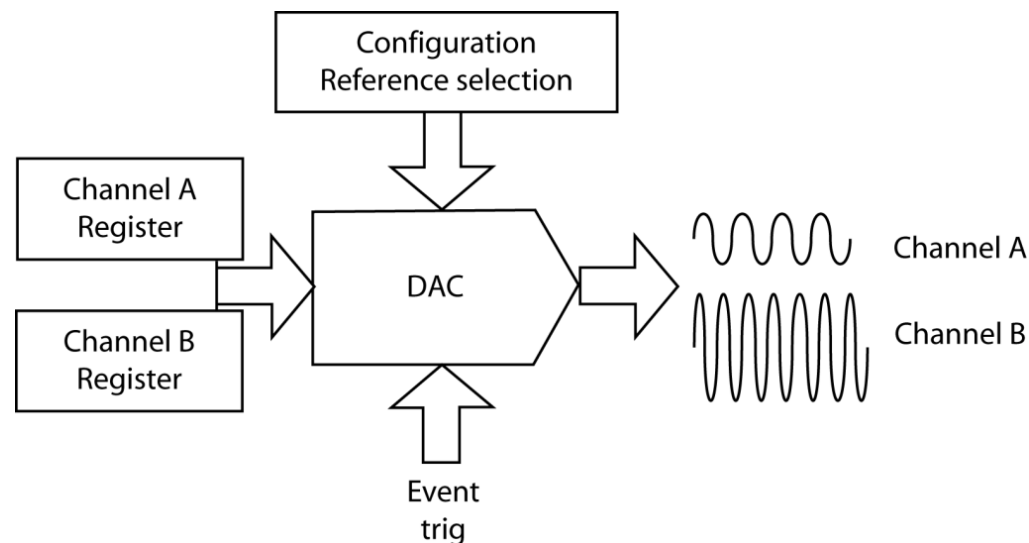


- n 4 virtual ADC channels
- n 8 – 12 external single-ended channels per ADC
- n 8 x 4 external differential channels per ADC
- n 4 internal channels
 - § VCC, Band gap, Temperature, DAC output
- n 1x, 2x, 4x, 8x, 16x, 32x or 64x gain
- n Synchronous sampling in dual ADC devices

XMEGA Digital to Analog Converter

n Features:

- § 12 Bit resolution
- § Up to 1 Msps conversion rate, 1 μ s settling time
- § Flexible conversion range (from 0V to up to $V_{CC}-0.3V$)
- § Connected to Event System
- § Connected to DMA Controller
- § 1 continuous or 2 S/H outputs



XMEGA Analog Comparators

n Selectable power vs. speed

- § 30 ns propagation delay in high-speed mode (130 μ A)
- § 20 μ A current consumption in low-power mode (500 ns)

n Selectable hysteresis

- § 0, 20mV, 50mV selectable

n Flexible input selections

- § Any analog input pin
- § Output of DAC module
- § Bandgap voltage reference
- § Scaled version of VCC

n Flexible interrupts and events generation

n Window compare function by combining 2 comparators

n Possible to have comparator output on a pin

XMEGA Timer/Counter

n Multiple 16-bit Timer/Counters in each device

- § Counts chip clock (Timer) or events (Counter)
- § 4 (2) Output Compare on each Timer/Counter
- § 4 (2) Input Capture on each Timer/Counter
- § Programmable Top Value
- § Direction control
- § Flexible interrupts and events generation

n High-Resolution Extension

- § 2x or 4x of chip clock = up to 128 MHz operation

n Advanced Waveform Extension

- § Inverted and Non-inverted PWM Outputs
- § Dead Time Insertion
- § Fault protection mechanism
- § Available in all devices, but on 1-2 timer/counters only

XMEGA Serial Communication Modules

n USART

- § Full duplex asynchronous or synchronous operation
- § Can also be SPI master
- § Baud Rate Generator with fractional divider
 - UART frequency crystals not needed

n SPI – Serial Peripheral Interface

- § Full duplex, three-wire synchronous data transfer

n TWI – Two Wire Interface

- § I²C compatible
- § SMBus compatible
- § Fast data rate on slow chip clock
 - Clock / 10 for master operation
 - Asynchronous slave operation

XMEGA Crypto engine

n AES

- § 128-bit key length
- § Encryption of 16 bytes in 375 clock cycles
- § Decryption of 16 bytes in 375 clock cycles

n DES

- § 56-bit key length
- § Encryption of 8 bytes in 16 clock cycles
- § Decryption of 8 bytes in 16 clock cycles

n Supports up to 1.25 Mbps AES encrypted communication

XMEGA Real Time Counter

n Separate Timer for Asynchronous Clock

- § Independent of other Timer/Counters
- § Works in Power Save, Idle and Active mode

n 16-bit timer with Programmable Prescaler

- § Prescaler provides 1 Hz – 32 kHz input
- § Programmable top value
- § Compare register
- § Max timeout 65 536 seconds (= more than 18 hours)

n Can generate Events and Interrupts

- § Both overflow and compare match

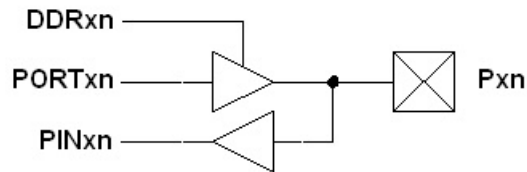
XMEGA Oscillators

- n 32 MHz internal RC oscillator**
 - § +/- 1% accuracy over temp, voltage and process
- n 2 MHz internal RC oscillator**
 - § +/- 1% accuracy over temp, voltage and process
- n 32 kHz internal RC oscillator**
 - § for low power operation
 - § +/- 2% accuracy over temp, voltage and process
- n 400 kHz – 16 MHz Crystal osc**
 - § for accurate timing in application
- n 32 kHz Crystal oscillator**
 - § for 32 kHz watch crystal
- n 32 kHz ULP RC oscillator**
 - § To be used by watchdog and brown-out detector
 - § 1mA power consumption
- n Internal PLL for high-freq clock generation**
 - § 400 kHz – 32 MHz input
 - § 8 – 128 MHz output
 - § Max 32 MHz output to main system clock

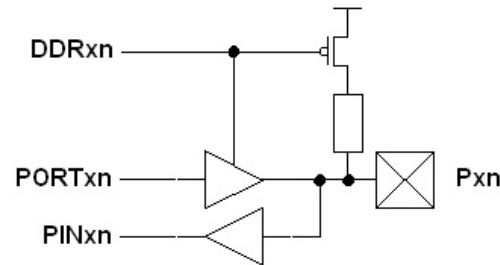
XMEGA I/O Pins

- n IN, OUT and DIR registers for safe read modify write operations
- n Virtual registers for easy pin manipulation
 - § Move IN, OUT and DIR control to bit addressable memory area
 - § Port Toggle, Clear and Set registers for easy and glitch free pin manipulation
- n Advanced pin configurations

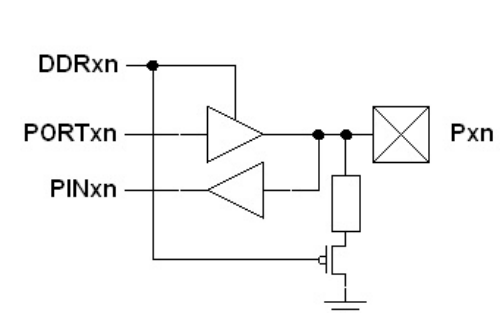
Push-pull



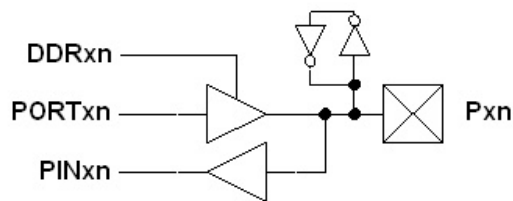
Push-pull w/pull-up



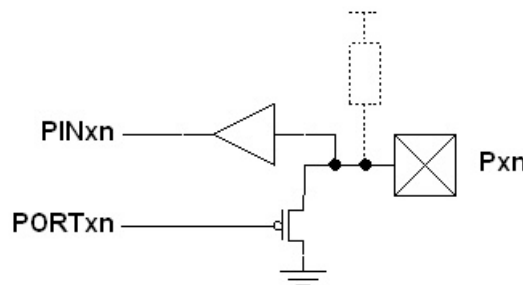
Push-pull w/pull-down



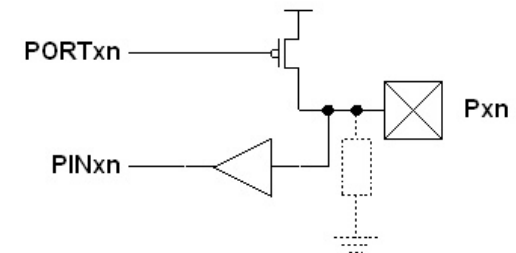
Push-pull w/ buskeeper



Wired AND w/ optional pull-up



Wired OR w/ optional pull-down



2nd generation picoPower

- n All picoPower features included
- n New sampled BOD
- n New low power Watchdog Timer
- n New Event system controls peripherals in Idle mode
- n New DMA moves data in Idle mode

n Lowest power consumption

- § 100 nA Power Down (RAM retention)
- § 650 nA Power Save (Real Time Clock)
- § 350 μ A 1 MHz Active
- § 3.6 mA 12 MHz Active
- § 2 μ s wake-up from Sleep modes



Sleep modes in XMEGA

- n 5 different sleep modes:**
- n Idle**
 - § All peripherals run as normal. No code can run
 - § Any peripheral can wake device
 - § DMA and Event system still working
- n Power save**
 - § Asynchronous clock operating. Only RTC can run
 - § Real Time Clock, External Interrupts, TWI Address Match and Watchdog Timer can wake the device
- n Power down**
 - § No clocks running. No operation
 - § External Interrupts, TWI Address Match and Watchdog Timer can wake the device
- n Standby**
 - § Power down, but oscillator is running for fast wake-up
- n Extended standby**
 - § Power save, but oscillator is running for fast wake-up

XMEGA Special Features

n Calibration memory

- § Readable from application
- § Factory calibration
- § User calibration
 - Can be modified by customer
- § Not affected by Chip Erase or SPM

n Serial numbers

- § Unique identifier
 - Lot ID, wafer#, X-Y coordinates
- § Random number seed

n Dynamic Clock Switching

n Oscillator failure detection

n Memory lock bits

n Brown-Out Detector

- § Very fast
- § Low power
- § Off, 1 kHz sampled or On

n Watchdog Timer

- § Separate oscillator

n Clock generation

- § Clock output

n CRC checksums

- § Available on locked devices

XMEGA Device Structure

n Analog – PORTA and PORTB

- § Analog to Digital Converter
- § Digital to Analog Converter
- § 2 Analog Comparators

n Digital – PORTC, PORTD, PORTE, PORTF

- § 2 16-bit Timer/Counters
 - AWeX on PORTC and PORTE
- § 2 USART
- § 1 Two Wire Interface (I²C and SMBus compatible)
- § 1 Serial Peripheral Interface (SPI)

n Memory interface – PORTH, PORTJ, PORTK, PORTL

- § SRAM and SDRAM

n Other modules exists in all devices

XMEGA Development Tools

n JTAG ICE mkII

- § JTAG or PDI debugging on XMEGA

n STK600

- § New starter kit for all AVR devices

n AVR ISP mkII

- § Low cost programmer

n AVR Studio

- § Simulator
- § On-Chip Debug emulator
- § C compiler support

n C compilers

- § IAR embedded workbench
- § WinAVR and GNU GCC



A4 subfamily

- 1 ADC 2 Msps
- 1 DAC
- 5 T/C
- 5 USART
- 2 SPI
- 2 TWI
- DMA
- Crypto

A3 subfamily

- 2 ADC 2 Msps
- 1 DAC
- 7 T/C
- 7 USART
- 4 SPI
- 2 TWI
- DMA
- Crypto

A1 subfamily

- 2 ADC 2 Msps
- 2 DAC
- 8 T/C
- 8 USART
- 4 SPI
- 4 TWI
- Ext Bus Interface
- DMA
- Crypto

384K

ATxmega384A1

256K

ATxmega256A3

ATxmega256A1

192K

ATxmega192A3

ATxmega192A1

128K

ATxmega128A4

ATxmega128A3

ATxmega128A1

64K

ATxmega64A4

ATxmega64A3

ATxmega64A1

32K

ATxmega32A4

16K

ATxmega16A4

44

64

100

XMEGA A1

n 2 12-bit 2 MSPS A/D Converters

§ 8 single ended channels

§ 8x4 differential channels with selectable gain

- 1/2/4/8/16/32/64x gain

n 2 12-bit DAC

n 4 Analog Comparators

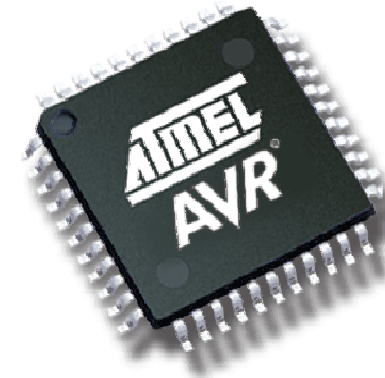
n 100-pin TQFP and CBGA

§ 78 General purpose I/O

n 8 16-bit Timer/Counters with Compare and Capture

n 8 USART, 4 TWI, 4 SPI

n External Bus Interface for SRAM and SDRAM



Device	Flash	RAM	E ²
ATXMEGA384A1	384K	32K	4K
ATXMEGA256A1	256K	16K	4K
ATXMEGA192A1	192K	16K	2K
ATXMEGA128A1	128K	8K	2K
ATXMEGA64A1	64K	4K	1K

XMEGA A3

n 2 12-bit 2 MSPS A/D Converters

§ 8 single ended channels

§ 8x4 differential channels with selectable gain

- 1/2/4/8/16/32/64x gain

n 1 12-bit DAC

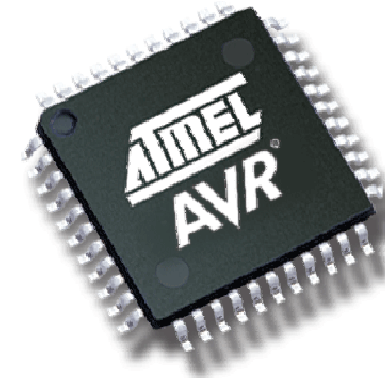
n 4 Analog Comparators

n 64-pin TQFP and QFN (MLF)

§ 50 General purpose I/O

n 7 16-bit Timer/Counters with Compare and Capture

n 7 USART, 2 TWI, 4 SPI



Device	Flash	RAM	E ²
ATXMEGA256A3	256K	16K	4K
ATXMEGA192A3	192K	16K	4K
ATXMEGA128A3	128K	8K	2K
ATXMEGA64A3	64K	4K	1K

XMEGA A4

n 12-bit 2 MSPS A/D Converters

§ 12 single ended channels

§ 8x4 differential channels with selectable gain

- 1/2/4/8/16/32/64x gain

n 1 12-bit DAC

n 2 Analog Comparators

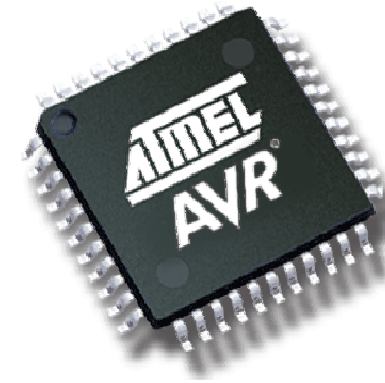
n 44-pin TQFP and QFN (MLF)

§ 34 General purpose I/O

n 5 16-bit Timer/Counters with

Compare and Capture

n 5 USART, 2 TWI, 2 SPI



Device	Flash	RAM	E ²
ATXMEGA128A4	128K	8K	2K
ATXMEGA64A4	64K	4K	1K
ATXMEGA32A4	32K	2K	1K
ATXMEGA16A4	16K	1K	1K