# megaAVR

Linecard & compatibility

AVR®

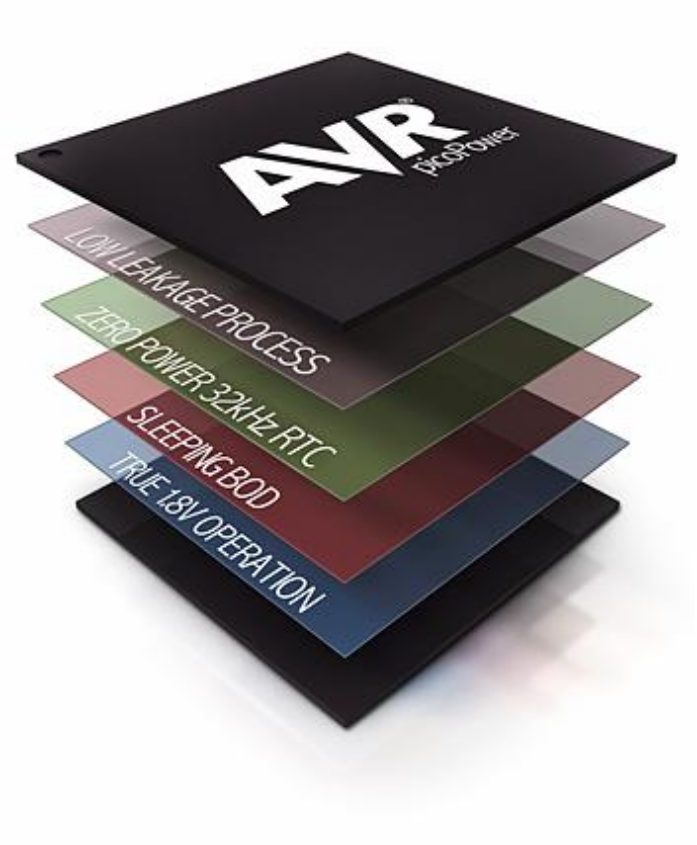
ATMEL®

# #1 in Performance, Power, Cost Trade-off

- Key differentiators:
  - Code density
  - Ease of Use
  - Read While Write Flash
  - JTAG
  - Safety Functions

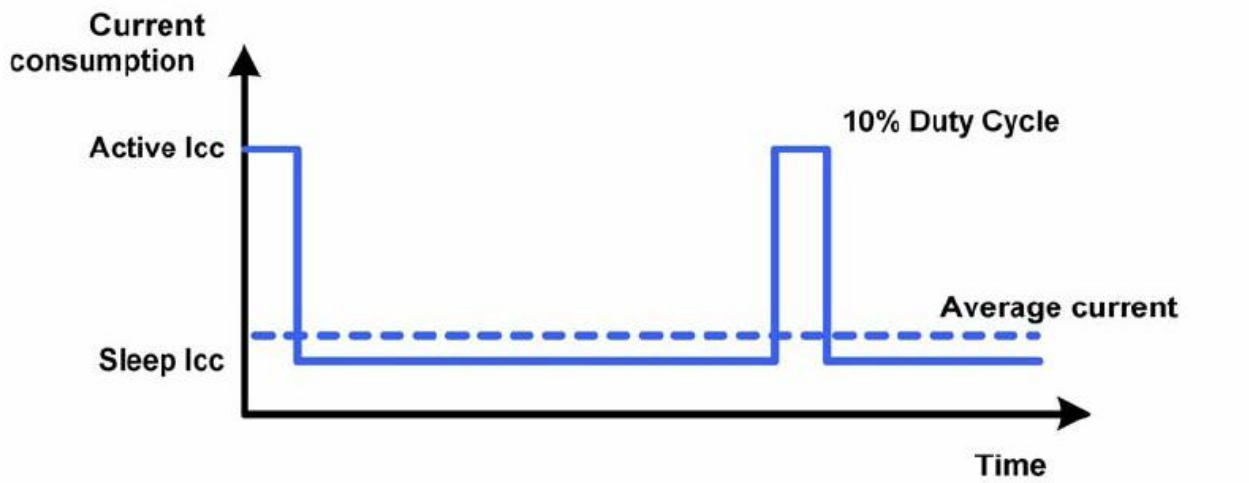
picoPower is #1 for high performance, low power applications

- Key elements:
  - Zero power 32kHz oscillator
  - Sleeping BOD
  - 1.8V operation
  - Power Reduction Register
  - Digital Input Disable Register
  - Low leakage process
  - Flash sampling



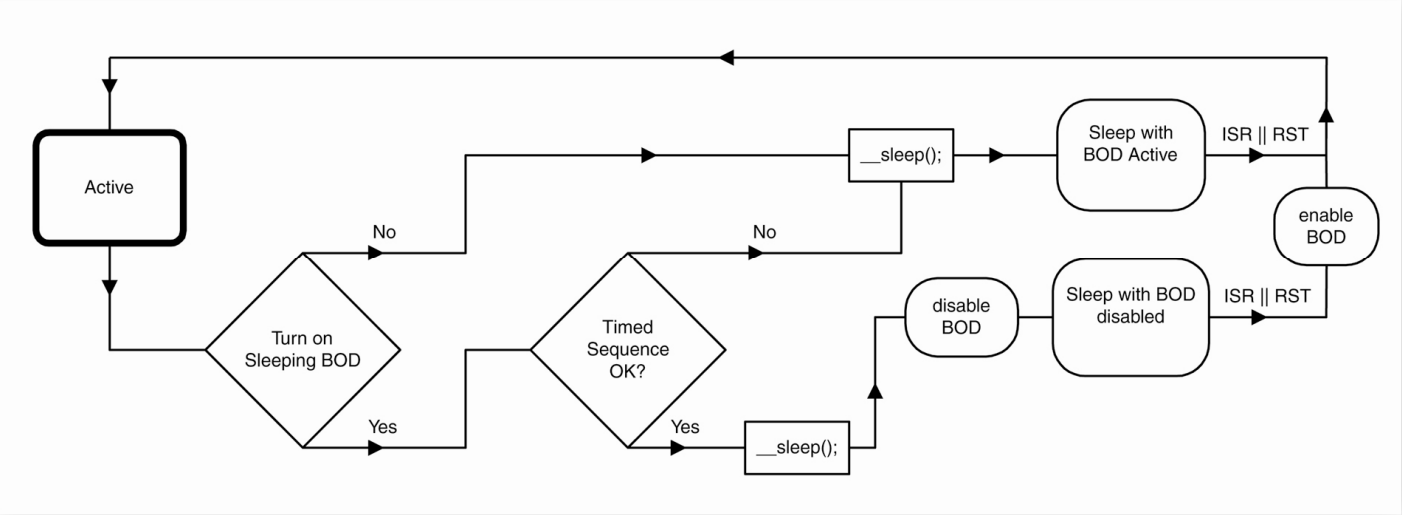
# Zero power 32kHz oscillator

- Brings Power-save current down to Power-down levels
  - 0.6uA Power Save mode @ 2.2V
- Most common wake up for low power applications is RTC
  - AVR picoPower 32 kHz oscillator uses ~300 nA
  - Wake up from sleep is either performed on reset or interrupts
  - Wakeup from sleep in 6 cycles
- Time in active is insignificant compared to time in Power-save



# Sleeping BOD

- BOD power consumption in sleep reduced to 0 nA
- Full BOD protection while in active mode
- No need for BOD in sleep
- BOD enters sleep right after the CPU and peripherals
- Automatically started upon wake-up
  - BOD starts first, then the rest of the AVR



# 1.8V operation

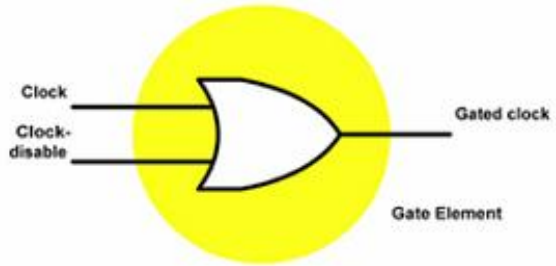
- True 1.8V operation ensures longer battery life time
  - Deeper discharge of batteries
  - Lower current consumption
- Power Consumption of a switching CMOS gate

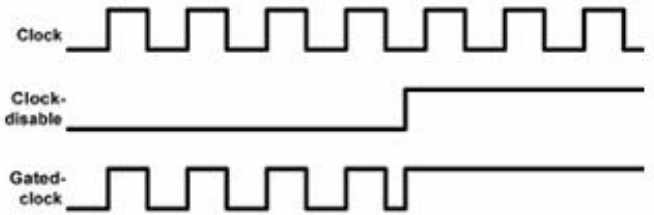
$$P_{dyn} = K \cdot V_{CC}^{2} \cdot f$$

- Low voltage operation challenges
  - Programming, reading, and retention of Flash and EEPROM
  - Reliable POR and BOD
- All challenges overcome
  - picoPower AVR fully operational from 1.8V

# Power Reduction Register

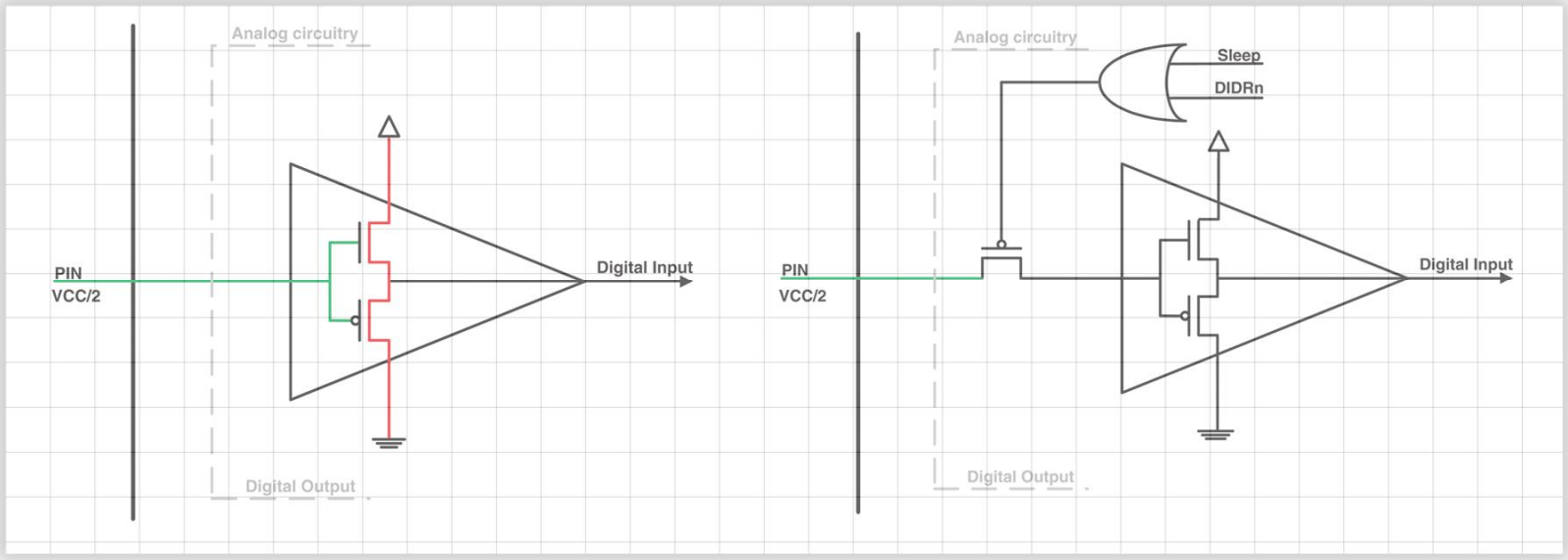
- No switching gates = no power consumption
  - PRR is the ultimate way to disable a module for any MCU
  - Normal disabling leaves the clock tree to the peripheral running
- Stops clock to individual peripherals
  - Peripheral is in PWD sleep while the rest of the device is running
- PRR accessible by application code



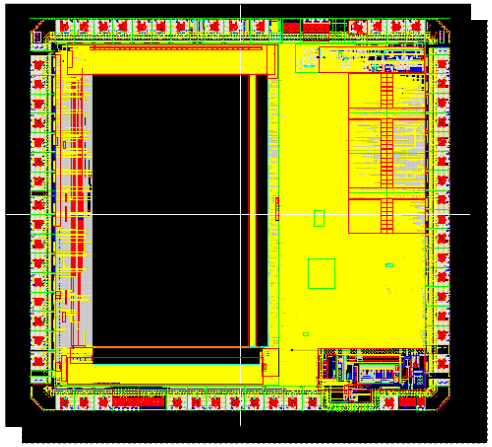
# Digital Input Disable Register

- Decreases power consumption
- Shuts off digital input buffers
- No power leakage
- Individual enable bit on all ADC pins
- Automatically enabled in sleep



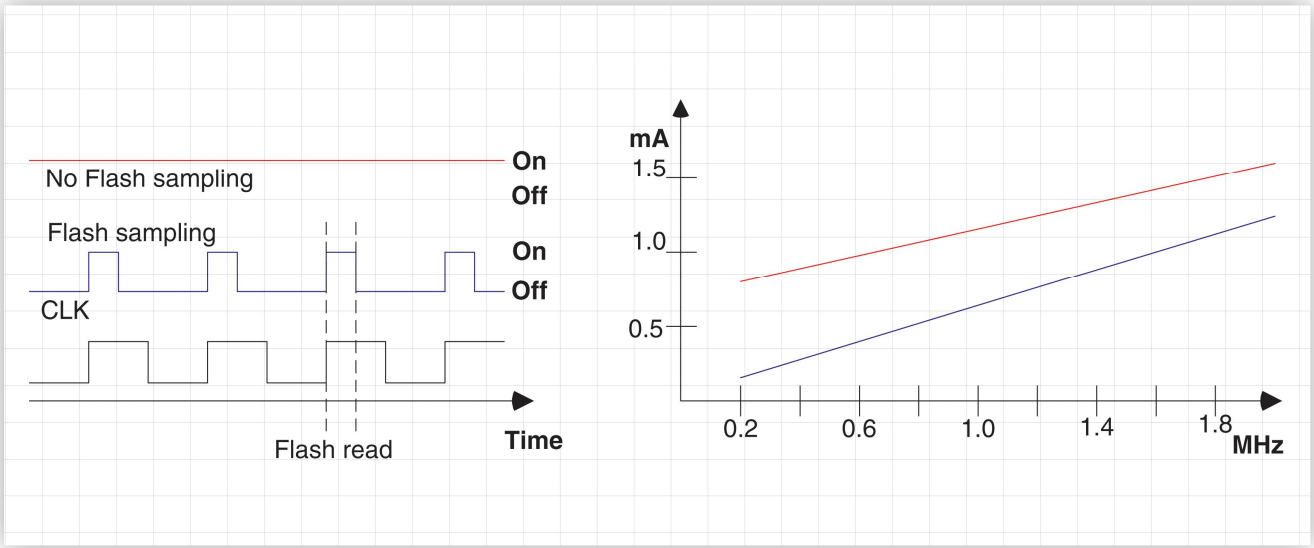
# Low leakage process

- Atmel has proprietary processes for low power operation
  - Enables down to 100nA current consumption in sleep
- Leakage is affected by:
  - Temperature
  - Supply voltage
  - Process
- Process is the only controllable factor
  - Rule of thumb; Smaller process gives higher leakage
  - Below 0.25 µm low leakage is very expensive
    - Process benefits are reduced

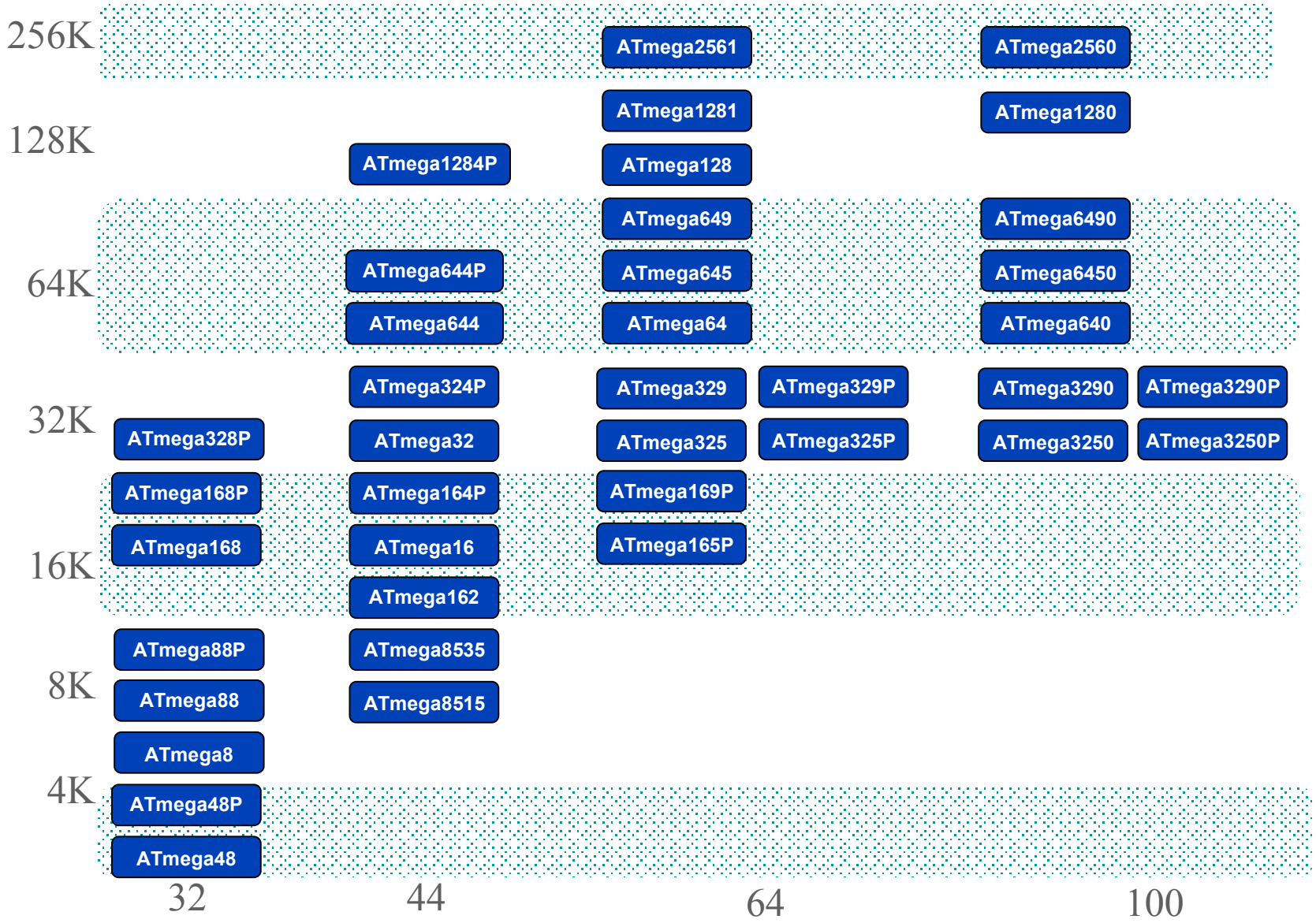


# Flash sampling

- Gives the most robust, and lowest power Flash
- Reading enables the Flash only a few nanoseconds
  - Independent of CPU frequency
- At low frequencies the read time is shorter than the clock cycle
- Flash arrays have static power consumption
  - Traditional Flash arrays are always powered

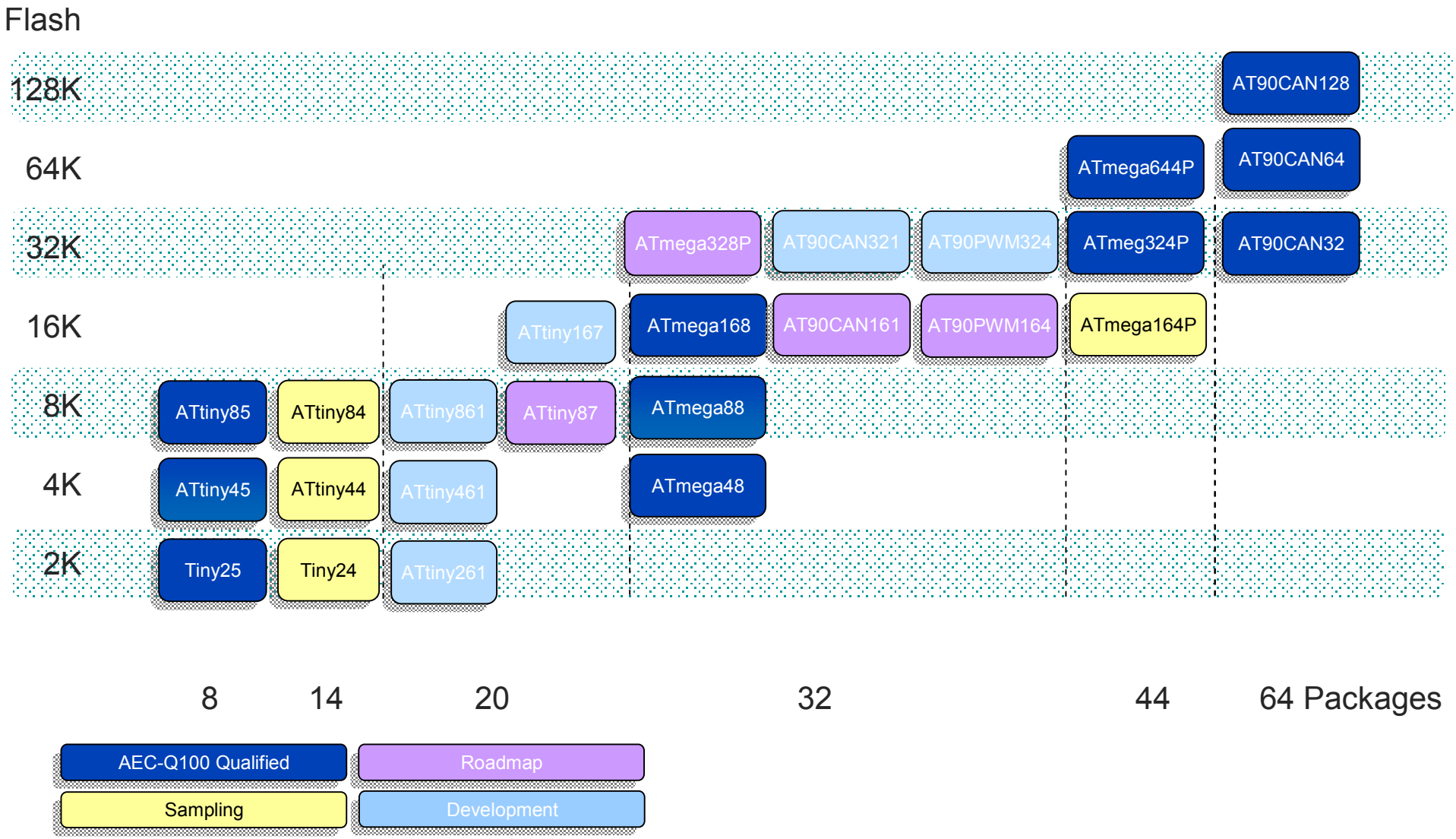


# Linecard


256K
128K
64K
32K
16K
8K
4K
ATmega2561
ATmega2560
ATmega1281
ATmega1280
ATmega1284P
ATmega128
ATmega649
ATmega6490
ATmega644P
ATmega645
ATmega6450
ATmega644
ATmega64
ATmega640
ATmega324P
ATmega329
ATmega329P
ATmega3290
ATmega3290P
ATmega328P
ATmega32
ATmega325
ATmega325P
ATmega3250
ATmega3250P
ATmega168P
ATmega164P
ATmega169P
ATmega168
ATmega16
ATmega165P
ATmega162
ATmega88P
ATmega8535
ATmega88
ATmega8515
ATmega8
ATmega48P
ATmega48
32
44
64
100

# Automotive AVR

# Automotive products portfolio




**AEC-Q100 grade 0 devices : ATtiny45, ATmega88**

- **Common features**
  - HW LIN/UART with clock adjust
  - CAN with 6 Message Objects
  - SPI Master/Slave
  - 100µA current source for hardware LIN address using single resistor
  - One 8 bits General purpose Timer/Counter
  - One 16 bits General purpose Timer/Counter
  - 10 bits ADC 120ksps
    - 11chan. single ended 3 chan. Diff.
  - 10 bits DAC
  - 4 Analog Comparators
  - On-chip Temperature sensor

| Device | Flash | RAM | $E^2$ | Pins |
|---|---|---|---|---|
| PWM324/CAN321 | 32K | 2K | 1K | 32 |

## PWM324 specific features

- 12-Bits Power Stage Controller
  - 6 complementary PWM outputs
  - Frequency up to 64MHz
  - Non-overlap protection
  - ADC synchronization
  - Fast Emergency stop
- PLL clock multiplier (up to 64MHz)

# Tiny167/87 LIN Controller

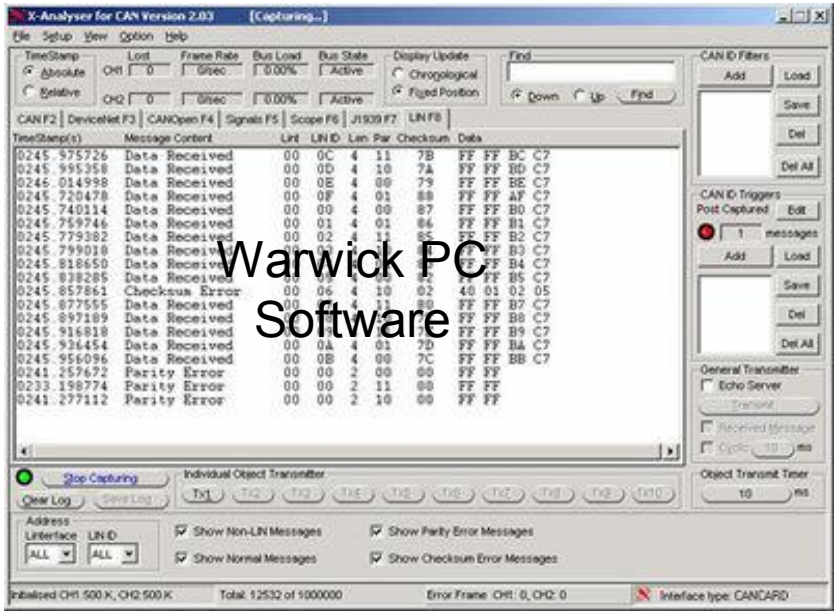
- **Features**
  - HW LIN/UART with clock adjust
  - 100µA current source for hardware LIN address using single resistor
  - USI Universal Serial Interface
  - SPI (Master and Slave)
  - Dynamic Clock switching
  - 10-Bits ADC 15ksps
    - 11 single ended channels
    - 8 diff. Channels with 1,8,20 gain
  - Analog Comparator
  - Programmable Voltage Reference

| Device | Flash | RAM | $E^2$ | Pins |
|---|---|---|---|---|
| ATtiny167 | 16K | 512 | 512 | 20 |
| ATtiny87 | 8K | 256 | 512 | 20 |

  - 1X 8-Bits Timer
  - 1X 16-Bit Timer
    - 2-channels PWM
  - Pin-Change interrupts
  - Watchdog
  - Low power modes

## ATAVRAUTO102 debugger kit

- ØDebugging Tool
- ØUSB connection to PC
- ØCAN Network monitoring
- ØCAN Network transmit
- Ø2 LIN Network Monitoring
- ØLIN 1 in Slave Only
- ØLIN 2 in Master / Slave




# ATAVRAUTO Evaluation Kit 1

Complete ready to use CAN/LIN network

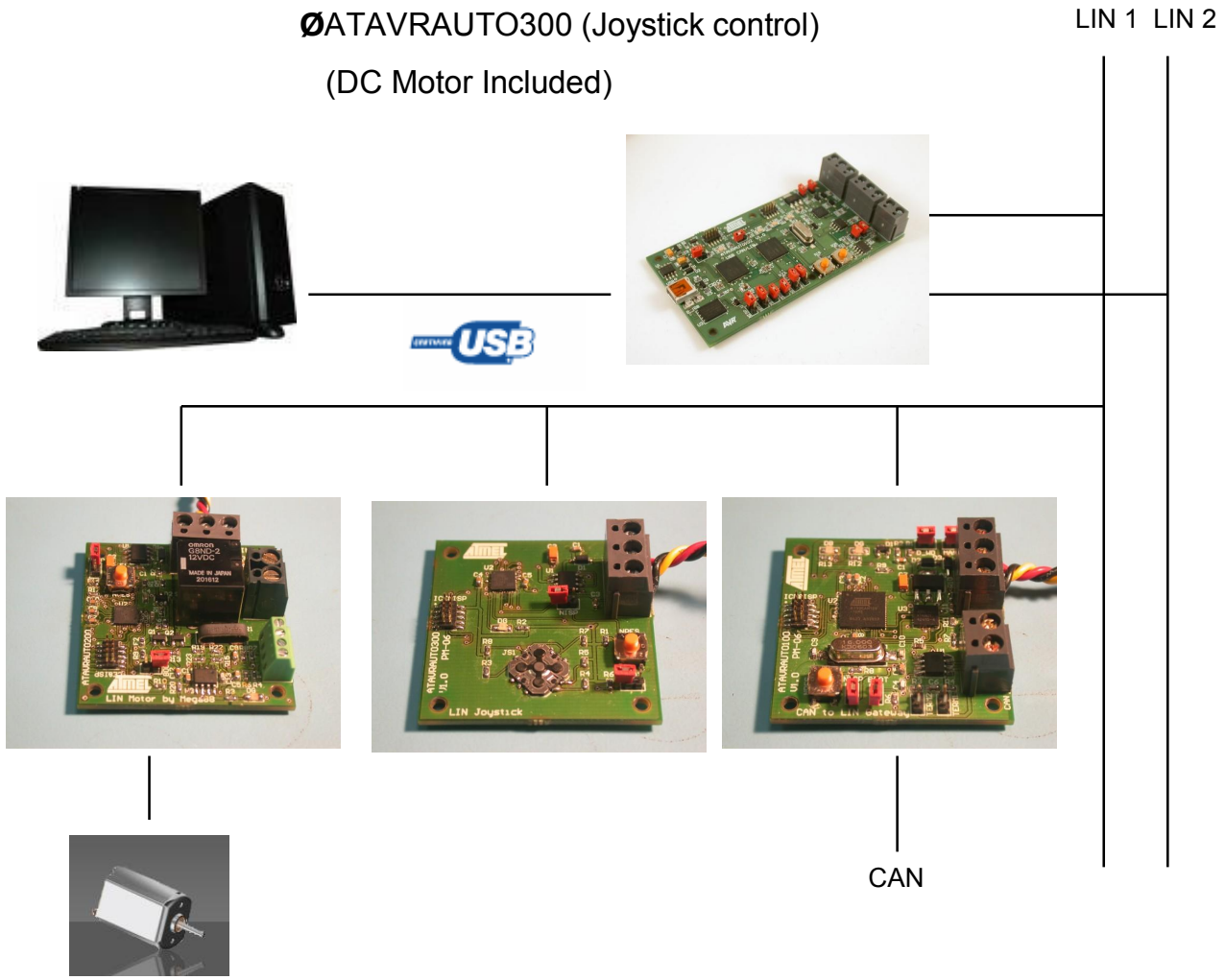
Kit Content

- Ø ATAVRAUTO102 (debugger tool)
- Ø ATAVRAUTO100 (Gateway CAN/LIN)
- Ø ATAVRAUTO200 (Motor Control)
- ØATAVRAUTO300 (Joystick control)

(DC Motor Included)

DC Motor control demo using joystick with Atmel LIN 1.3 Libraries

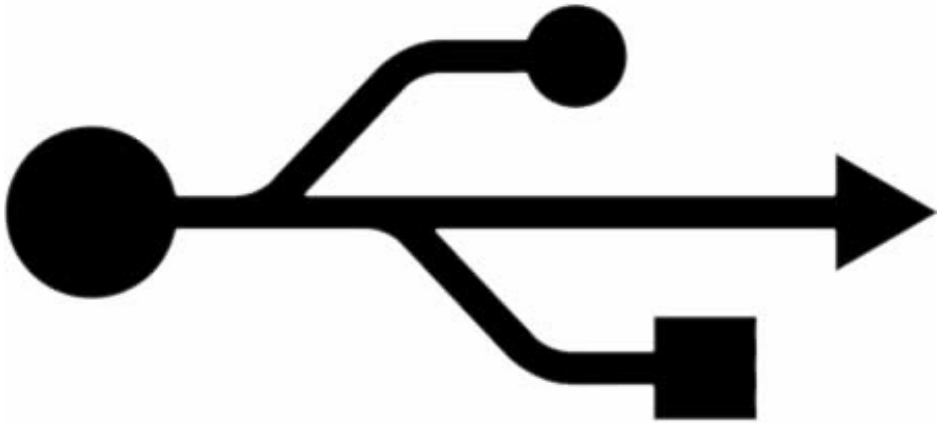
CAN/LIN Gateway implemented on ATAVRAUTO100



# ASSP AVR


# USB

| Device | Flash | RAM | EE | USB | VCC |
|---|---|---|---|---|---|
| AT90USB326 | 32K | 2K | 1K | USB | 2.7-5.5V |
| AT90USB324 | 32K | 2.5K | 1K | USB | 2.7-5.5V |
| AT90USB164 | 16K | 1K | 512 | USB | 2.7-5.5V |
| AT90USB82 | 8K | 512 | 512 | USB/PS2 | 2.7-5.5V |
| AT90USB162 | 16K | 512 | 512 | USB/PS2 | 2.7-5.5V |



# PWM

| Device | Flash | RAM | EE | PWM | I/0 |
|---|---|---|---|---|---|
| AT90PWM1 | 8K | 512 | 512 | 7 | 19 |
| AT90PWM216 | 16K | 1K | 512 | 7 | 19 |
| AT90PWM316 | 16K | 1K | 512 | 10 | 27 |

- AT90PWM1
  - No DALI
- AT90PWM216/316
  - Indentical to AT90PWM2/3, but
  - Double Flash and RAM